F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 10

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Release Date:	Dec. 10, 2008
Due Date	**:** Dec. 17, 2008

1 Today's Laboratory Objective

Practice how to design and simulate memory logic.

2 Background

For information about how to use Cadence tool, jump to the following tutorials:

- Cadence general introduction:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/`
- Cadence delay setting:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/DelaySetting.html`
- Logic circuit glossary:
  `http://www.u-aizu.ac.jp/~benab/classes/ld/doc/glossary.html`

2.1 Basic Types of Digital Circuits

The basic **and**, **or**, and **not** gates can be combined in a huge variety of ways to build the digital circuitry that drives modern computers. Two basic categories of circuits are:

Combinational Circuits: Circuits whose outputs depend only on the current inputs; hence they appear to combine the inputs in some way to produce the outputs; and
Sequential Circuits: Circuits whose outputs depend on the both the current and past inputs; hence they use the sequence of inputs over time to determine the output.

3 Exercise 10-1: RS NOR latch Design

Refer to Fig. 1.

1. Draw the schematic

Table 1: Gates delay assumption.

TYPE	Function	DELAY
INV	Inverter	1
AND2	2 input AND	2
AND3	3 input AND	3
AND4	4 input AND	4
OR2	2 input OR	2
OR3	3 input OR	3
OR4	4 input OR	4
NOR2	2 input NOR	2
NOR3	3 input NOR	3
XOR2	2 input XOR	3
XOR3	3 input XOR	4

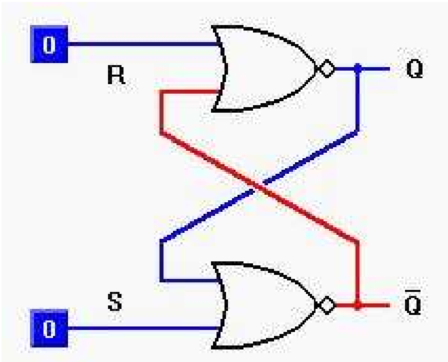

Figure 1: RSFF from NOR's.

2. Set delay for each logic. Use the given gate library in Table 1.
3. Make a symbol
4. Write down testfixture to simulate the test sequences:
   RS = 10, 00,01,00,11 and 00
5. Simulate the circuit and explain the behaviours of RS NOR latch.

4 Exercise 10-2: Master-slave DFF Design

Refer to Figure 2.

1. Draw the schematic
2. Set delay for each logic. Use the given gate library in Table 1.
3. Make a symbol
4. Write down testfixture. Initially assign 0 to C and D. Then, change C every 50ns and D every 100ns.
5. Simulate the circuit and explain the behaviours of DFF.

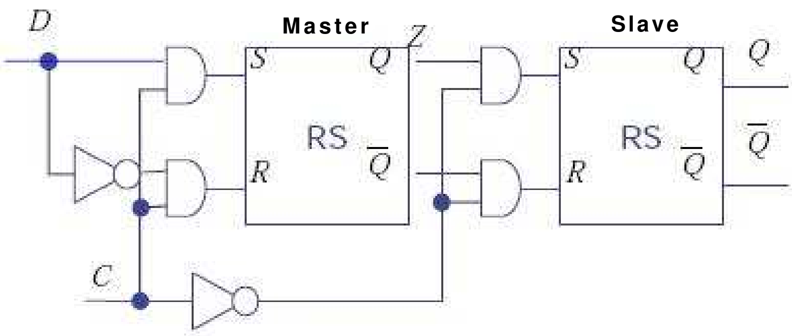

Figure 2: Master Slave DFF.

5 Exercise 10-3: Positive edge-trigger DFF Design

Refer to Figure 3.

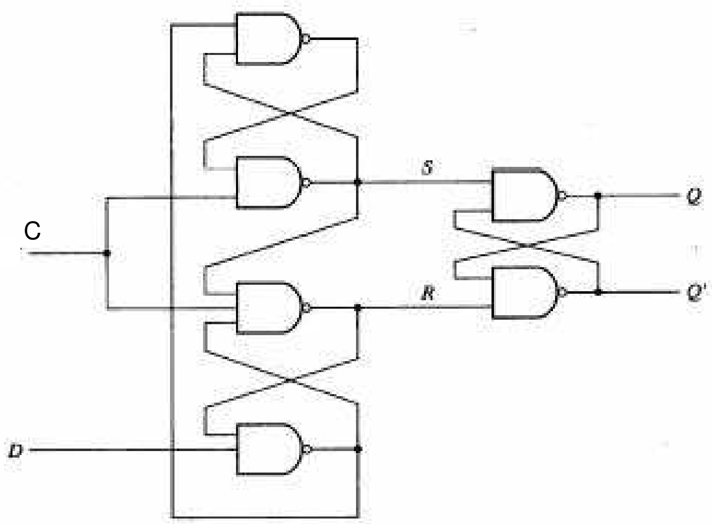

Figure 3: Positive Edge-trigger DFF circuit.

1. Draw the schematic
2. Set delay for each logic. Use the given gate library in Table 1.
3. Make a symbol
4. Write down testfixture. Initially assign 0 to C and D. Then, change C every 50ns and D every 100ns.
5. Simulate the circuit and explain the behaviours of DFF.

6 Exercise 10-3: 16-bit Register Design

Refer to Figure 4.

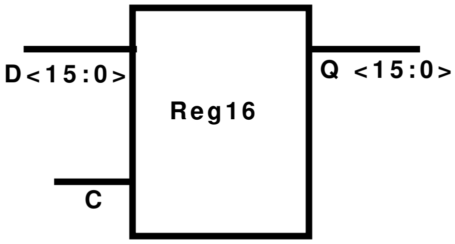

Figure 4: 16-bit Register symbol.

1. Draw the schematic
2. Make the symbol
3. Write down testfixture to simulate the register by assigning D with 16'h0000, 16'hffff, 16'h0f0f, and 16'habcd. Change C every 50ns.
4. Simulate the circuit and explain when input data appears to output.

7 Report submission

7.1 Contents

Your report should be prepared in English and should contain the following:

- Your name, your ID and the Lab #.

For Exercises 10-1, 10-2, 10-3, submit the following:

- Schematic (with gate delay)
- Testfixure.new
- Waveform and explanation.

For Exercise 10-4, submit the following:

- Schematic
- Testfixure.new
- Waveform and explanation.

7.2 Submission Format

Hard Copy.

References

[1] Hiroshi Saito, Logic Circuit Design Course Web page, Second Semester, 2008.