F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 12

Ben A. Abderazek
The University of Aizu
E-mail:benab@u-aizu.ac.jp

Release Date:	Jan. 7, 2009
Due Date :	Jan. 14, 2009

1 Today's Laboratory Objective

Learn how to design a finite state machine (FSM).

2 Background

For information about how to use Cadence tool, jump to the following tutorials:

- Cadence general introduction:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/`
- Cadence delay setting:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/DelaySetting.html`
- Logic circuit glossary:
  `http://www.u-aizu.ac.jp/~benab/classes/ld/doc/glossary.html`

2.1 Finite State representation of digital circuits

2.1.1 Finite State Machine (FSM)

A finite state machine (FSM) is a model of behavior composed of a finite number of states, transitions between those states, and actions.
In general any synchronous circuit can be modelled by a finite state machine, and vice versa.

2.1.2 Why use finite state machines?

- The finite state machines give us a way specifying exactly what a circuit should do.
- Having designed the finite state machine we can apply a design methodology to create the actual circuit.
- FSMs play a crucial role in CS as a modelling tool.

Table 1: Gates delay assumption.

TYPE	Function	DELAY
INV	Inverter	1
NAND2	2 input NAND	2
NAND3	3 input NAND	3
NOR2	2 input NOR	2
NOR3	3 input NOR	3
AND2	2 input AND	3
AND3	3 input AND	4
OR2	2 input OR	3
OR3	3 input OR	4
XOR2	2 input XOR	5
XOR3	3 input XOR	6

2.2 Sequential Circuit Design Methodology (Lab 12 too)

Refer to Fig. 1.

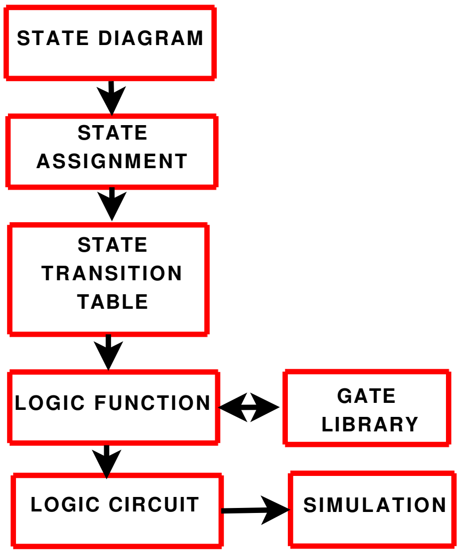

Figure 1: Sequential Circuit Design Methodology (Lab 12 too)

3 Exercise 12-1: Vending machine controller design

Design a vending machine controller using Moore machine. Refer to Fig. 1. The behaviors of the controller are defined as follows:

1. Accepts either 50 yen or 100 yen at a time
2. Coffee is issued when 150 yen is injected
3. The state of the controller is initially set to 0 yen by a reset signal. Use master-slave DFF with a reset signal.

4. The state is changed whenever the positive edge of clock signals happens
5. The controller works repeatedly when surplus exists

3.1 Exercise 12-1 Tasks

- Define inputs, outputs, and states
- Write down the state diagram (state transition graph) for the FSM
- Perform state assignment
- Write down the state transition table and output table
- Synthesize logic circuits for the state transition function and the output signals
- Draw schematic and set delay
- Decide clock cycle time
  1. Analyze the critical path delay of a circuit for the state transition function
  2. We assume setup time, hold time, and marging as 10 ns, 10 ns, and 20 ns respectively (40 ns in total).
  3. Calculate the clock cycle time 1+2
- Write down testfixture.new so that all state transitions are simulated
- Simulate the circuit and explain the correctness of the circuit (Simulate all state transitions).

4 Exercise 12-2 (Extra)

Redesign the controller using Mealy machine.

4.1 Exercise 12-2 Tasks

- Define inputs, outputs, and states
- Write down the state diagram (state transition graph) for the FSM
- Perform state assignment
- Write down the state transition table
- Synthesize logic circuits for the state transition function and the output signals
- Draw schematic and set delay
- Decide clock cycle time
  1. Analyze the critical path delay of the circuit for the state transition function
  2. We assume setup time, hold time, and merging as 10 ns, 10 ns, and 20 ns respectively (40 ns in total).
  3. Calculate the clock cycle time 1 + 2
- Compare the number of used gates and the clock cycle time between Moore machine and Mealy machine.

- Write down testfixture.new so that all state transitions are simulated
- Simulate the circuit and explain the correctness of the circuit (Simulate all state transitions).

5 Report submission

5.1 Contents

Your report should be prepared in English and should contain the following:

- Your name, your ID and the Lab #.

For Exercises 12-1 submit the following:

- FSM (state diagram and mathematical representation)
- State assignment
- State transition table targeting for the master-slave DFF
- Logic functions derived from Karnaugh map
- Logic circuit
- Schematic (with delays)
- Explanation how to decide clock cycle time
- Testfixture.new
- Waveform and explanation

For Exercise 12-2, submit the following:

- FSM (state diagram and mathematical representation)
- State assignment
- State transition table targeting for the master-slave DFF
- Logic functions derived from K map
- Logic circuit
- Schematic (with delays)
- Explanation how to decide clock cycle time
- Comparision between Moore and Mealy machines.
- Testfixture.new
- Waveform and explanation.

5.2 Submission Format

Hard Copy.

References

[1] Hiroshi Saito, Logic Circuit Design Course Web page, Second Semester, 2008.