F4 - Logic Circuit Design Exercises

2nd Semester, 2008

Lab 7

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Release Date: Nov. 12, 2008
Due Date : Dec. 3 , 2008

1 Today's Laboratory Objective

Practice how to design and simulate combinational circuits.

2 Background

For information about how to use Cadence tool, jump to the following tutorials:

- Cadence general introduction:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/`
- Cadence delay setting:
  `http://www.u-aizu.ac.jp/~benab/classes/ca/doc/cadence/DelaySetting.html`
- Logic circuit glossary:
  `http://www.u-aizu.ac.jp/~benab/classes/ld/doc/glossary.html`

Table 1: Gates delay assumption.

TYPE	Function	DELAY
INV	Inverter	1
AND2	2 input AND	2
AND3	3 input AND	3
AND4	4 input AND	4
OR2	2 input OR	2
OR3	3 input OR	3
OR4	4 input OR	4
XOR2	2 input XOR	3
XOR3	3 input XOR	4

Table 2: 2-to-1 MUX

In1	In2	Sel	Out
0	*	0	0
1	*	0	1
*	0	1	0
*	1	1	1

Table 3: 4-to-1 MUX

In1	In2	In3	In4	Sel	Out
0	*	*	*	00	0
1	*	*	*	00	1
*	0	*	*	01	0
*	1	*	*	01	1
*	*	0	*	10	0
*	*	1	*	10	1
*	*	*	0	11	0
*	*	*	1	11	1

2.1 Basic Types of Digital Circuits

The basic **and**, **or**, and **not** gates can be combined in a huge variety of ways to build the digital circuitry that drives modern computers. Two basic categories of circuits are:

Combinational Circuits: Circuits whose outputs depend only on the current inputs; hence they appear to combine the inputs in some way to produce the outputs; and

Sequential Circuits: Circuits whose outputs depend on the both the current and past inputs; hence they use the sequence of inputs over time to determine the output

In this lab, we only practice the first category - *combinationa circuit*.

3 Exercise 7-1: Multiplexer Design

Refer to Figure 1(a) and the thruth tables shown in Tables 2 and 3, then design 2-to-1 and 4-to-1 multiplexers.

- Derive logic functions from Tables 2 and 3.
- Draw schematics using the defined library.
- Make symbol.
- Find the number of gates and the critical path delay.
- Write down testfixures by using Tables 2 and 3.
- Simulate circuits and verify the correctness using waveform.

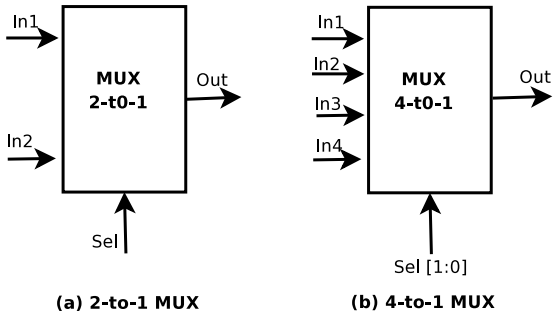

Figure 1: MUX symbol.

4 Exercise 7-2: 3-to-8 Decoder Design

Refer to Figure 2 and design 3-to-8 decoder.

- Write down the truth table.
- Derive logic functions.
- Draw schematic using the defined library.
- Make symbol.
- Find the number of gates and the critical path delay.
- Write down testfixure so that all input combinations are simulated.
- Simulate circuit and verify the correctness using waveform.

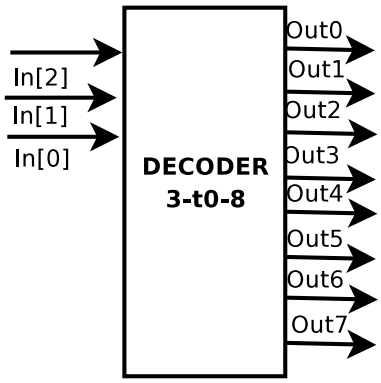

Figure 2: Decoder symbol.

5 Exercise 7-3: Full Adder Design

Refer to Figure 3(a) and design a full adder.

- Write down the truth table.
- Derive logic functions using K map.
- Draw schematic using the defined library.

Table 4: Test sequences

A[15:0]	B[15:0]	addsub	S[15:0]
0101	L4DID	0	
00ff	L4DID	0	
0f0f	L4DID	0	
ffff	L4DID	0	
0101	L4DID	1	
00ff	L4DID	1	
0f0f	L4DID	1	
ffff	L4DID	1	

- Make the symbol.
- Find the number of gates and the critical path delay.
- Write down testfixure so that all input combinations are simulated.
- Simulate the circuit and verify its correctness using waveform.

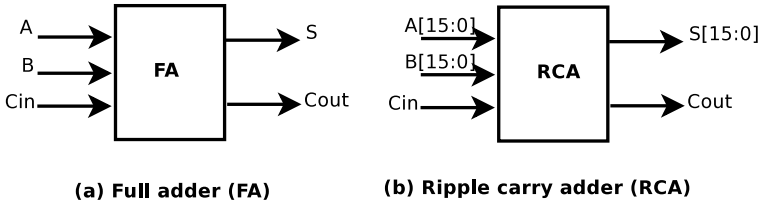

Figure 3: FA and RCA symbols.

6 Exercise 7-4: 16-bit Ripple Carry Adder (RCA) Design

Refer to Figure 3(b) and design a 16-bit ripple carry adder.

- Draw schematic using desined full adders.
- Make symbol.
- Find the number of gates and the critical path delay.
- Write down testfixure to simulate the test sequences shown in Table 4.
  Set B[15:0] to the last four digits of your ID (L4DID) (i.e. s1140155 $->$ 0155).
- Simulate the circuit and verify its correctness using waveform.

7 Report submission

7.1 Contents

Your report should be prepared in English and should contain the following:

1. Your name, your ID and the Lab #.
2. **Exercise 7-1**
   - Truth table for 2-to-1 and 4-to-1 multiplexers.
   - Logic functions for 2-to-1 and 4-to-1 multiplexer.
   - Schematics (with gate delay).
   - The number of gates and the critical path delay for 2-to-1 and 4-to-1 multiplexers.
   - Testfixture.new for 2-to-1 and 4-to-1 multiplexers.
   - Waveforms.
3. **Exercise 7-2**
   - Truth table for 3-to-8 decoder.
   - Logic functions for 3-to-8 decoder.
   - Schematic (with gate delay).
   - The number of gates and the critical path delay.
   - Testfixture.new.
   - Waveform.
4. **Exercise 7-3**
   - Truth table for full adder.
   - Logic functions with Karnaugh maps.
   - Schematic (with gate delay).
   - The number of gates and the critical path delay.
   - Testfixture.new.
   - Waveform.
5. **Exercise 7-4**
   - Schematic (with gate delay).
   - Number of gates and critical path delay.
   - Testfixture.new.
   - Waveform.

7.2 Submission Format

Hard Copy.

References

[1] Hiroshi Saito, Logic Circuit Design Course Web page, Second Semester, 2008.