Adaptive Systems Research

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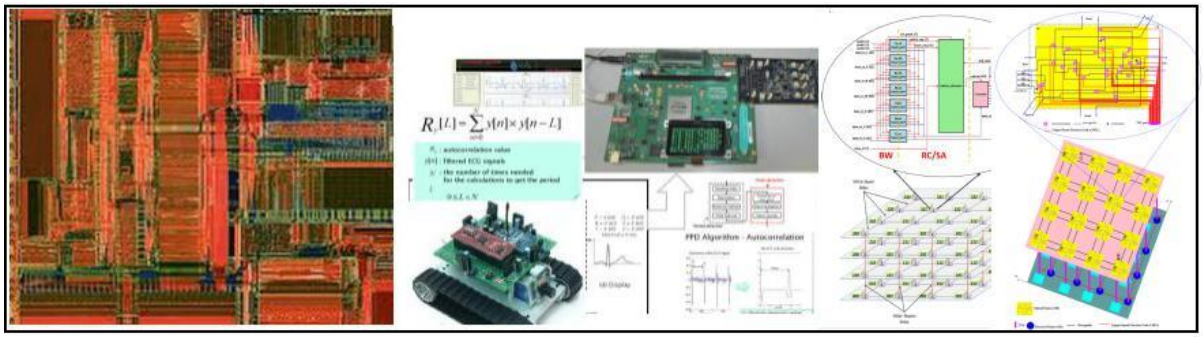
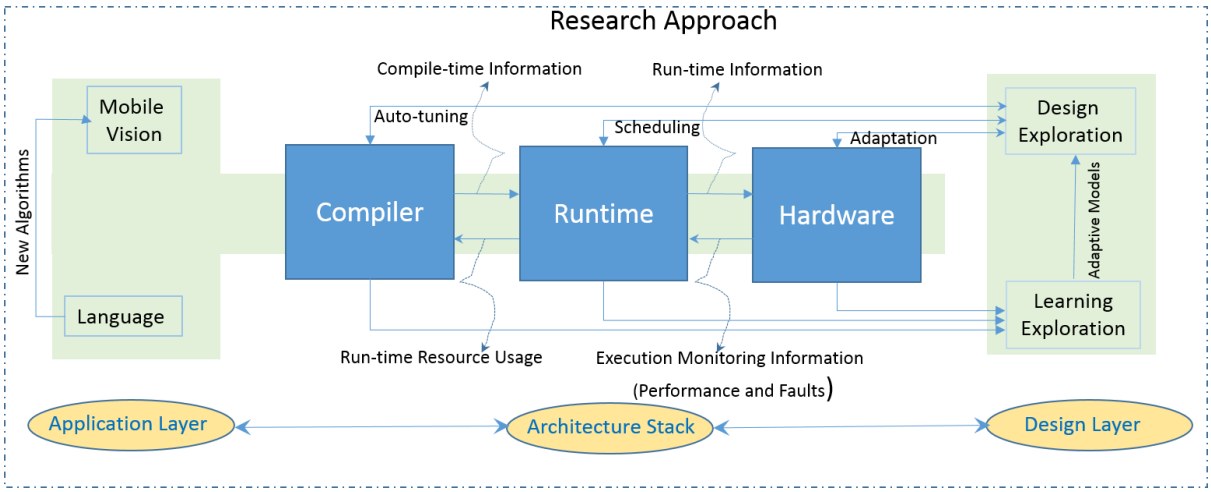
Abstract

The main focuses of the Adaptive Systems Laboratory are mainly on research and education of new methodologies and novel architectures for current and emerging technologies, and microelectronic devices. These devices form the core technology for communications and personal computing, industry, business, defense, etc. For such devices, there is a need for efficient error detection, diagnosis and recovery protocols. There is also a need for architectures that can combine fault tolerance aspects with performance aspects in an adaptive manner, adapting to different runtime environments and different user requirements. For these goals, we explore adaptive hardware configurations, novel low-power design methodologies and architectures, and adaptive algorithms for the design of a reliable systems. Our recent research projects include self-adaptive microprocessor, architecture design for robust system resilient to permanent and transient faults, and Highly-reliable Intra- and Inter-Chip Network-on-Chip for future Many-core Systems.



High-Performance, Low-power, and Fault-tolerant Heterogenous Many-core Systems



Highly-reliable Intra- and Inter-Chip Interconnection Networks

PHENIC: Silicon-Photonics Network-on-Chip for Low-power, High-throughput Many-core Systems

The huge computing power of many-core multi-processor systems will require very large on-chip and off-chip data transfer rates (> 100TB/s). One efficient technology for transmitting this level of information is the optical interconnects, which promise significant advantages over their electronic counterparts. In particular, optical on-chip interconnect (ONoC)) offers a potentially disruptive technology solution with fundamentally low power dissipation that remains independent of capacity while providing ultra-high throughput and minimal access latency. In addition, when combined with 3D integration technology, ONoC offers advantages over 2D NoC design, such as shorter wire length, higher packing density, and smaller footprint [1,2,3,4,5].

Our ASL team will build a sophisticated hybrid electronic-photonic interconnect layer including microsources, photodetectors and different advanced wavelength routing functions. We will demonstrate the application of such electornic-photonic ICs in on-chip optical network. Our approach which inherits several promising features from our earlier proposed OASIS 3D-NoC, offers low-latency data propagation and ultra-wide bandwidth by leveraging wavelength-division multiplexing (WDM) and time-division multiplexing (TDM). The final goal is is to provide a compact, low-power-consumption, high bandwidth and low-latency photonic on-chip interconnection network with full CMOS-compatibility.

OASIS: Scalable Packet-Switched Network-on-Chip Architecture for Multicore Systems

Future System-on-Chip (SoC) will contain hundreds of components made of processor cores, DSPs, memory, accelerators, and I/O all integrated in a single die area of just a few square millimeters. Such small and complex SoC will be interconnected via a novel on-chip interconnect closer to a sophisticated network than to current bus-based solutions. This network must provide high throughput and low latency while keeping area and power consumption low. Our research effort is about solving several design challenges to enable such new NoC paradigm in many-core systems. In particular, we are investigating implementation techniques for basic building blocks, new topologies, flow control techniques, and low-latency, high-throughput/fault-tolerant routing algorithms [1-24]

Adaptive System Design and Manycore SoC Design for Real-time Bio-medical and Vision-based Object Localization and Recognition Applications

Many ubiquitous applications, such as bio-medical, vision-based object localization and recognition or ADAS applications, are characterized by complex and data-intensive computations which complicate the task of achieving real-time performance on today's technology. Power efficiency is also a real challenge if these applications are run on battery powered mobile systems. Since there is no single architecture that is capable of fulfilling all these requirements, such systems require some kind of adaptivity. This means systems should monitor themselves, analyze their own behavior, and adapt to several execution environments.

The goal of this research, which combines the developed algorithms and techniques from our other two topics, is to research and develop new algorithms and techniques for a power-efficient and real-time system which exploits (whenever possible) all kinds of

parallelism (ILP, DLP, TLP and multicore). Our target is computation intensive applications, such bio-medical and object-recognition applications. This includes coordinated tasks on all system components ranging from core level architecture, to compiler and runtime systems, all the way to hardware techniques. Such an approach naturally requires bidirectional data flow and information exchange between components, and therefore new set of dynamic interfaces between the individual components, as well as adaptivity within each module [21,15,7].

BANSMOM: Real-Time Multicore System for Remote Monitoring of Elderly Health

OASIS-VP: Research and Development of Vision Processor

With the advance in microprocessor technology, demands for practical vision and image recognition applications have been appearing in automobile, security, surveillance, and robot applications. Processing multi-objects recognition require higher computing power, making it difficult to perform the computation on conventional shared bus general-purpose processors, despite the recent dramatic improvements in processor performance. Therefore, specialized architecture for communication and computation are needed for high-performance image recognition tasks. Three dimensional Networks-on-Chip (3D-NoC) has been proposed as a promising architecture which combines the high parallelism of Network-on-Chip (NoC) interconnect paradigm with the high-performance and lower interconnect-power of 3-dimensional integration circuits. However, as 3D-NoCs keep showing their advantages against 2D-NoC architectures, their reliability is put under question

The main goal of this project is to research about algorithms and, architecture for a high-performance vision processor. The system is based on our earlier developed reliable Network-on-Chip (OASIS). We will first research about efficient algorithm for recognition of multi-objects in real-time. Then, we will perform research about novel architecture which can effectively detect, diagnosis, and recover from large number of transient faults in the proposed vision processor. This study should cover all the system components that are most susceptible to failure such as inter-router links, input-buffer, and the crossbar. At the end of this research, the final design should be implemented on a real chip.

SEA: Self-Adaptive Processor

This research is about a novel computing model and architecture based on an innovative self-adaptation behavior, which will provide scalability, high resource utilization, and high-performance by dynamically synthesizing the right resources composition based on temporal program performance demand(s). A given program is considered as a set of small objects competing with other programs running on the same many-core platform. In this computing model, a given program can dynamically occupy/find new space and spread/migrate its computation (various parallelism levels) to appropriate neighbour cores. Using our dynamic temporal-allocation-technique, a given program can de-allocate resources according to its new performance requirement [51].

Architecture and Micro-architecture of Low-power, High-performance Microprocessors

Research on Energy-aware Scheduling and Resource Allocation in Cloud Computing Systems

A cloud computing system is essentially a large-scale distributed computing system consisting of large heterogeneous hardware and software resources (components). Cloud computing is characterized by its scalable resource allocation for various

applications/Workloads. This characteristic can be realized by virtualization technologies with many-core processors. We are investigatigating the problem of energy-aware scheduling and resource allocation schemes for different workloads exploiting power consumption characteristics of heterogeneous many-core processors.

Low-power High-performance Queue Computer

Future systems will expose a huge amount of parallelism requiring +1000 cores. As a result, current programming models and applications cannot be used to exploit these terascale systems. Our aim in this research is to propose a complete solution that can exploit the terascale parallelism efficiently. We are researching in both hardware and software sides. In the software side, we are focusing on the programming model, compiler optimizations. On the hardware side, we are focusing on a scalable architecture using available execution cores and interconnection networks. Our previous work on Data-flow Queue computing principles are again re-visited in this research and exploited at all levels to overcome the current limitations of traditional control-flow model [34-123].

Reliable Concurrent VLSI@ASL

References

1. Ben Abdallah (Author), "Multicore Systems-on-Chip: Practical Hardware/Software Design, 2nd Edition" , Publisher: Springer/Atlantis, 2013, ISBN-13: 978-9491216916.
2. Ben Abdallah (Author), "Multicore Systems-On-Chip: Practical Hardware/Software Design", Publisher: World Scientific/Atlantis, 2010, ISBN 978-90-78677-22-2. A. Ben Abdallah (Editor and one of the authors), "Multicore Systems on Chips", Publishers: Signpost, 2007, ISBN: ISBN 978-81-7895-258-1.
3. Ben Abdallah,"On-Chip Optical Interconnects: Prospects and Challenges, Invited Talk", 6th International Conference of Soft Computing and Pattern Recognition, August 11-14, 2014.
4. Ben Ahmed, M. Meyer, Y. Okuyama, and A. Ben Abdallah, "Adaptive Error- and Traffic Aware Router Architecture for 3D Network-on-Chip Systems ", IEEE Proceedings of the 8th International Symposium on Embedded Multicore/Many-core SoCs (MCSoC-14), pp. 197-2014, Sept. 2014.
5. Ben Ahmed, A. Ben Abdallah, "OASIS 3D-Router Hardware Physical Design", Technical Report, Adaptive Systems Laboratory, Division of Computer Engineering, School of Computer Science and Engineering, University of Aizu, July 8, 2014.
6. Ben Ahmed, A. Ben Abdallah, "Graceful Deadlock-Free Fault-Tolerant Routing Algorithm for 3D Network-on-Chip Architectures", Journal of Parallel and Distributed Computing, 74/4 (2014), pp. 2229-2240.
7. Achraf Ben Ahmed, A. Ben Abdallah, "Architecture and Design of Real-Time System for Elderly Health Monitoring", Journal of Embedded Systems, 2014.
8. Ben Ahmed, A. Ben Abdallah, "PHENIC: Towards Photonic 3D-Network-on-Chip Architecture for High-throughput Many-core Systems-on-Chip", IEEE Proc. of the 14th Int. Conf. on Sciences and Techniques of Automatic Control and Computer Eng., Dec. 2013.
9. Akram Ben Ahmed, Achraf Ben Ahmed, A. Ben Abdallah, "Deadlock-Recovery Support for Fault-tolerant Routing Algorithms in 3D-NoC Architectures", IEEE Proceedings of the 7th International Symposium on Embedded Multicore/Many-core SoCs (MCSoC-13), pp. 67-72, 2013.
10. Akram Ben Ahmed, A. Ben Abdallah, "Architecture and Design of High-throughput, Low-latency and Fault Tolerant Routing Algorithm for 3D-Network-on-Chip", The Jnl. of Supercomputing, December 2013, Volume 66, Issue 3, pp 1507-1532.
11. Achraf Ben Ahmed, A. Ben Abdallah, "Hardware/Software Prototyping of Dependable Real-Time System for Elderly Health Monitoring", IEEE Proc. of the World Congress on Computer and IT (ICMAES), June 2013.

12. Akram Ben Ahmed, T. Ouchi, S. Miura, A. Ben Abdallah, "Run-Time Monitoring Mechanism for Efficient Design of Application-specific NoC Architectures in Multi/Manycore Era", IEEE Proc. of the 6th International Workshop on Engineering Parallel and Multicore Systems (ePaMuS2013), July 2013.
13. Ben Abdallah, "Towards the Development of Smart Multicore Bio-Chip for Body-Area Networks ", Invited tak, IEEE-PCSJ Conference, November 2, 2013.
14. Ben Abdallah, "PHENIC: Silicon Photonic 3D-Network-on-Chip Architecture for High-performance Heterogeneous Many-core System-on-Chip ", Technical Report, Adaptive Systems Laboratory, The University of AizuRef. PTR0901A0715-2013, Sept. 013.
15. Achraf Ben Ahmed, "Interactive Real-time Interface for Smart Remote Health Monitoring and Analysis ", Master's Thesis, Graduate School of Computer Science and Engineering, The University of Aizu, Feb. 2013.
16. Kenichi Mori, "OASIS Network-on-Chip Prototyping on FPGA ", Master's Thesis, The University of Aizu, Feb. 2012.
17. Akram Ben Ahmed, "On the Design of a 3D Network-on-Chip for Many-core SoC ", Master's Thesis, The University of Aizu, Feb. 2012.
18. Akram Ben Ahmed, A. Ben Abdallah, "On the Design of a 3D Network-on-Chip for Many-core SoC ", Technical Report, The University of Aizu, Feb. 2012.
19. Akram Ben Ahmed, A. Ben Abdallah, "Low-overhead Routing Algorithm for 3D Network-on-Chip ", IEEE Proc. of the The Third International Conference on Networking and Computing (ICNC'12), pp. 23-32, 2012.
20. Akram Ben Ahmed, A. Ben Abdallah, "LA-XYZ: Low Latency, High Throughput Look-Ahead Routing Algorithm for 3D Network-on-Chip (3D-NoC) Architecture ", IEEE Proceedings of the 6th International Symposium on Embedded Multicore SoCs (MCSoC-12), pp. 167-174, 2012.
21. Achraf Ben Ahmed, Yumiko Kimezawa, A. Ben Abdallah, "Towards Smart Health Monitoring System for Elderly People ", IEEE Proceedings of The 4th International Conference on Awareness Science and Technology (iCAST 2012), pp. 248-253, 2012.
22. Akram Ben Ahmed, A. Ben Abdallah, "ONoC-SPL Customized Network-on-Chip (NoC) Architecture and Prototyping for Data-intensive Computation Applications ", IEEE Proceedings of The 4th International Conference on Awareness Science and Technology (iCAST 2012), pp. 257-262, 2012.
23. Ryuya Okada, "Architecture and Design of Core Network Interface for Distributed Routing in OASIS NoC", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2012.
24. Tomotaka Kasahara, "Performance and Complexity Study of Multi-QueueCore Systems", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2012.
25. R. Okada, "Architecture and Design of Core Network Interface for Distributed Routing in OASIS NoC", Technical Report, Adaptive Systems Lab, The University of Aizu, Feb., 2012.
26. Ben Abdallah, et al., "Natural Instruction Level Parallelism-aware Compiler for High-Performance QueueCore Processor Architecture", Journal of Supercomputing, Vol. 57, No. 3 (2011), pp. 314-338.
27. Hiroki Hoshino, "Development of Parallel Queue Processor Architecture and its Integrated Development Environment", Master's Thesis, Graduate School of Computer Science and Engineering, The University of Aizu, Feb. 2011.
28. Taichi Maekawa, "Design and Evaluation of Dual Mode Processor Architecture", Master's Thesis, Graduate School of Computer Science and Engineering, The University of Aizu, Feb. 2011.
29. Masashi Masuda, "Produced Order Queue Compiler Design", Master's Thesis, Graduate School of Computer Science and Engineering, The University of Aizu, Feb. 2011.
30. Takahiro Uesaka, "OASIS NoC Topology Optimization with ShortPath Link", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2011.
31. Shunichi Kato, "Shared Memory MultiQueueCore Processor Design", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2011, Ref. 10SK-GT10.
32. Yumiko Kimezawa, "Multicore SoC Architecture for Realtime Data Intensive ECG Processing", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2011.

33. Akram Ben Ahmed, A. Ben Abdallah, K. Kuroda, Architecture and Design of Efficient 3D Network-on-Chip (3D NoC) for Custom Multicore SoCs, IEEE Proc. of the 5th International Conference on Broadband, Wireless Computing, Communication and Applications (BWCCA-2010), Nov. 2010.
34. K. Mori, A. Esch, A. Ben Abdallah, K. Kuroda, Advanced Design Issues for OASIS Network-on-Chip Architecture, IEEE Proc. of the 5th International Conference on Broadband, Wireless Computing, Communication and Applications (BWCCA-2010), Nov. 2010, pp. 74-79.
35. Ben Abdallah, Efficient Parallel ECG Processing Algorithm and Design of Flexible Health Monitoring System for Elderly People, Innovation Research Journal, March 2010, pp. 24-27.
36. Ben Abdallah, Y. Haga, K. Kuroda, "An Efficient Algorithm and Embedded Multicore Implementation for ECG Analysis in Multi-lead Electrocardiogram Records", IEEE Proc. of the 39th he International Conference on Parallel Processing Workshop, San Diego, pp.99-103, Sept. 13-16, 2010.
37. Yuuki Omoto, "Development Environment for Single Chip Computer intended for Queue Computing Development and Education", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2010.
38. Haga Yasuyoshi, "Architecture and Design of Application Specific Multicore SoC", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2010.
39. Reo Honjoya, "Development of User Friendly Assembler for Queue Computers", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2010.
40. Mori Kenichi, "Optimizations Techniques and FPGA Prototyping of OASIS Network-on-Chip", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2010.
41. Miura Shohei, "Architecture and Design of Parameterizable Network-on-Chip", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2010.
42. Y. Haga, A. Ben Abdallah, and K. Kuroda, "Embedded MCSoC Architecture and Period-Peak Detection (PPD) Algorithm for ECG/EKG Processing", 'The 19th Intelligent System Symposium (FAN 2009), pp.298-303, Sep. 2009.
43. S. Miura, A. Ben Abdallah, and K. Kuroda, "PNoC - Design and Preliminary Evaluation of a Parameterizable NoC for MCSoC Generation and Design Space Exploration", The 19th Intelligent System Symposium (FAN 2009), pp.314-317, Sep. 2009.
44. K. Mori, A. Ben Abdallah, and K. Kuroda, "Design and Evaluation of a Complexity Effective Network-on-Chip Architecture on FPGA", The 19th Intelligent System Symposium (FAN 2009), pp.318-321, Sep. 2009.
45. M. Masuda, A. Canedo, A. Ben Abdallah, "Efficient Code Generation Algorithm for Natural Instruction Level Parallelism-aware Queue Architecture", The 19th Intelligent System Symposium (FAN 2009), pp.308-313, Sep. 2009.
46. Canedo, A. Ben Abdallah, and M. Sowa, "Efficient Compilation for Queue Size Constrained Queue Processors", The Journal of Parallel Computing, Vol.35, pp. 213-225, 2009.
47. Canedo, A. Ben Abdallah, and M. Sowa, "Compiler Support for Code Size Reduction using a Queue-based Processor", Transactions on High-Performance Embedded Architectures and Compilers, Vol. 2, Issue 4, pp. 269-285, 2009.
48. Shohei Miura, Abderazek Ben Abdallah, Kenichi Kuroda, "設計空間探索とMCSoCの生成に適している parameterizable NoC (PNoC)のハードウェア設計と事前評価", 第34回パル テノン研究会, pp.105-108, Aug. 2009.
49. Masashi Masuda, "Graph Transformation Methods and Theoretical Performance Evaluation of Queue Computation Models ", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2009.
50. Hiroki Hoshino, "Advanced Hardware Optimization Algorithms for High Performance Queue Processor Architecture ", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2009.
51. Tachi Maekawa, "Research on Hardware Design of Dual-Mode Processor Architecture", Bachelor Thesis, School of Computer Science and Engineering, The University of Aizu, Feb. 2009.
52. A Canedo, A. Ben Abdallah, M Sowa, "Design and implementation of a queue compiler", Jnl of Microprocessors and Microsystems 33 (2), pp.129-138, 2009.

53. Masashi Masuda, A Ben Abdallah, Arquimedes Canedo, "Software and Hardware Design Issues for Low Complexity High Performance Processor Architecture", IEEE Prof. of the Int. COnference of Parallel Processing Workshops, pp. 558-565, 2009.
54. Ben Abdallah, A. Canedo, T. Yoshinga, and M. Sowa, The QC-2 Parallel Queue Processor Architecture, Journal of Parallel and Distributed Computing, Vol. 68, No. 2, pp. 235-245, 2008.
55. T. Maekawa, A. Ben Abdallah, and K. Kuroda, "Single Instruction Dual-Execution Model Processor Architecture", Proc. IEEE/IFIP Int'l Conf. on Embedded and Ubiquitous Computing (EUC2008), pp.30-36, Dec. 2008.
56. H. Hoshino, A. Ben Abdallah, and K. Kuroda, "Advanced Optimization and Design Issues of a 32-bit Embedded Processor Based on Produced Order Queue Computation Model", IEEE/IFIP Int'l Conf. on Embedded and Ubiquitous Computing (EUC2008),pp.16-22, Dec.2008.
57. Canedo, A. Ben Abdallah, and M. Sowa, "Quantitative Evaluation of Common Subexpression Elimination on Queue Machines", Proc. IEEE Int'l Sym. on Parallel Architectures, Algorithms, and Networks (I-SPAN 2008), pp.25-30. 2008.
58. Ben Abdallah, et. all, "Processor for Mobile Applications", ISBN: 978-1-60566-046-2, IGI Publishers, 2008.
59. M. Akanda, A. Ben Abdallah, and M. Sowa, "Dual-Execution Mode Processor Architecture", Journal of Supercomputing, Vol. 44, No. 2, pp. 103-125, 2008.
60. M. Sowa. et all. "Queue Machines for Next Generation Computer Systems", Proc. of The International Workshop on Modern Science and Technology (IWMST), 2008.
61. Canedo, Ben Abdallh Abderazek, and Masahiro Sowa, "Compiling for Reduced Bit-Width Queue Processors", Journal of Signal Processing Systems,Volume 59, Issue 1, pp 45-55, 2010.
62. Canedo, A. Ben Abdallah, and M. Sowa, "A New Code Generation Algorithm for 2-offset Producer Order Queue Computation Model", Journal of Computer Languages, Systems & Structures, Vol. 34, Issue 4, pp. 184-194, 2007.
63. Ben Abdallah, and M. Sowa, "Advanced Power Management Techniques for Mobile Communication Systems", Journal of Computer Research, Vol. 14, No.2 , pp. 109-128, 2007.
64. Mushiq Akanda, A. Ben Abdallah, and M. Sowa, "Dual-Execution Mode Processor Architecture for Embedded Applications", Journal of Mobile Multimedia, Vol. 3, No. 4, pp. 347-370, 2007.
65. Y. Nakanishi, A. Canedo, A. Ben Abdallah, and M. Sowa, "Optimizing Reaching Definitions Overhead in Queue Processors", Journal of Convergence Information technology, 2007, Vol. 2, No. 4, pp. 36-40, 2007.
66. Ben Abdallah, and M. Sowa, "Efficient Design Methodology and Synthesizable Core for Multicore SoCs", ISBN: 978-81-7895-258-1, Signpost Publishers, 2007.
67. Ben Abdallah, and M. Sowa, "Buffer Design in Packet Switched Networks for MCSoCs Applications", ISBN: 978-81-7895-258-1, Signpost Publishers, 2007.
68. Ben Abdallah, and M. Sowa, "Power Optimization techniques for Mobile Multicore SoCs", ISBN: 978-81-7895-258-1, Signpost Publishers, 2007.
69. Canedo, A. Ben Abdallah, M. Sowa, New Code Generation Algorithm for QueueCore An Embedded Processor with High ILP, IEEE Proc of the Eighth International Conference on Parallel and Distributed Computing, Applications and Technologies, 185-192, 2007.
70. Ben Abdallah , T Yoshinaga, and M. Sowa, "Mathematical Model for Multiobjective Synthesis of NoC Architectures", IEEE Proc. of the 36th International Conference on Parallel Processing, Sept., 2007.
71. Canedo, A. Ben Abdallah, and M. Sowa, "Queue Register File Optimization Algorithm for QueueCore Processor", Proc. IEEE 19th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2007), pp. 169-176, 2007.
72. Canedo,A. Ben Abdallah, and M. Sowa, "An Efficient Code Generation Algorithm for Code Size Reduction using 1-offset P-Code Queue Computation Model", Proc. IFIP International Conference on Embedded and Ubiquitous Computing (EUC07), pp. 196-208, 2007.
73. Canedo, A. Ben Abdallah, and M. Sowa, "Compiler Framework for an Embedded 32-bit Queue Processor", Proc. of the International Conference on Convergence Information Technology (ICCIT07), Gyeongju, South Korea, pp. 877-884, 2007.
74. Yuki, T.; Canedo, A.; Abderazek, B.A.; Sowa, M., "Novel Addressing Method for Aggregate Types in Queue Processors," Convergence Information Technology, 2007. International Conference on , vol., no., pp.1793,1796, 21-23 Nov. 2007.

75. Arquimedes Canedo, Ben Abdallah Abderazek, and Masahiro Sowa, "Queue Compiler Development", IPSJ-SIGPRO, 2007-2-(10).
76. Ben Abdallah, T. Yoshinaga, and M. Sowa, "High-Level Modeling and FPGA Prototyping of Produced Order Parallel Queue Processor Core", Journal of supercomputing, Vol. 38, Number 1, pp. 3-15, 2006.
77. Ben Abdallah, Sotaro Kawata, and M. Sowa, "Design and Architecture for an Embedded 32-bit QueueCore", Journal of Embedded Computing, Special Issue in embedded single-chip multicore architectures, Vol. 2, No. 2, pp. 191-205, 2006.
78. Ben Abdallah, and M. Sowa, "Advanced Power Reduction Techniques in Mobile Computing Systems", ISBN:1-60021-207-7, Nova Science Publishers, 2006.
79. Ben Abdallah, T. Yoshinaga, and M. Sowa, "Scalable Core-Based Methodology and Synthesizable Core for Systematic Design Environment in Multicore SoC (MCSoC)", Proc. IEEE 35th International Conference on Parallel Processing Workshops, Aug. 14-18th, pp. 345-352, 2006.
80. Ben Abdallah, Masahiro Sowa, Basic Network-on-Chip Interconnection for Future Gigascale MCSoCs Applications: Communication and Computation Orthogonalization, Proc. of the Symposium on Science, Society, and Technology (TJASSST2006), pp. 4-6, 2006/12.
81. Musfiquzzaman, A. Ben Abdallah, and M. Sowa, "On the Design of a Dual-Execution Modes Processor: Architecture and Preliminary Evaluation", Frontiers of High Performance Computing and Networking – ISPA 2006 Workshops, Lecture Notes in Computer Science Volume 4331, 2006, pp 37-46.
82. Arquimedes Canedo, Ben Abdallah Abderazek, and Masahiro Sowa, "A GCC-based Compiler for the Queue Register Processor (QRP-GCC)", The International Workshop on Modern Science and Technology 2006.
83. TQ Viet, T Yoshinaga, A. Ben Abdallah, M Sowa, "Construction of Hybrid MPI-OpenMP Solutions for SMP Clusters", Prof. of Information and Media Technologies 1 (1), pp.45-57, 2006.
84. T. Viet, T. Toshinaga ,A. Ben Abdallah, and M. Sowa, "Construction of Hybrid MPI-OpenMP Solutions for SMP Clusters", IPSJ transactions on Advanced Computing Systems, Vol.46, pp.25-37, Jan. 2005.
85. M. Sowa, A. Ben Abdallah, and T. Yoshinaga, "Processor Architecture Based on Produced Order Computation Model", Journal of Supercomputing, Vol. 32,No. 3, pp. 217-229, June 2005.
86. Ben Abdallah, M. Arsenji, S. Shigeta, T. Yoshinaga, and M. Sowa, "Modular Design Structure and High-Level Prototyping for Novel Embedded Processor Core", Proc. of International Conference on Embedded and Ubiquitous Computing (EUC2005), LNCS Vol.3824, pp. 340-349, 2005.
87. M. Akanda, A. Ben Abdallah, S. Kawata, and M. Sowa, "An Efficient Dynamic Switching Mechanism (DSM) for Hybrid Processor Architecture", Proc. of International Conference on Embedded and Ubiquitous Computing (EUC2005), LNCS Vol.3824, pp. 77-86, Dec. 2005.
88. Markovskij, A. Ben Abdallah, S. Kawata, and M. Sowa, "Architecture of Produced-order Parallel Queue Processor: Preliminary Evaluation", Proc. of the 38th International Symposium on Microarchitecture (MICRO-38), Nov. 2005.
89. Ben Abdallah, T. Yoshinaga, and M. Sowa, "Rapid FPGA Prototyping of a Queue Processor Core for Embedded Computing", Proc. of 67th Conf. of Information Processing Society of Japan, March 2~4, 2005.
90. Ta Quo Viet, T. Yoshoinaga, and A Ben Abdallah, "Performance Enhancement for Matrix Multiplication on an SMP PC Cluster", Summer United Workshops on Parallel, Distributed and Cooperative Processing, August 2005.
91. Ben Abdallah, Markov Arsenji, S. Shigeta, T. Yoshinaga, and M. Sowa, "Queue Processor for Novel Queue Computing Paradigm Based on Produced Order Scheme", Proc. IEEE of the 7th High Performance Computing and Grid in Asia Pacific Region (HPCAsia2004), pp. 169-177, July 2004.
92. Shigeta, L.-Q. Wang, N. Yagishita, A. Ben Abdallah, T. Yoshinaga, and M. Sowa, "QJava: Integrate Queue Computational Model into Java", Proc. of the Joint Japan-Tunisia Workshop on Computer Systems and Information Technology (JT-CSIT'04), July 2004.
93. Markovskij, M. Sowa, A. Ben Abdallah, S. Shigeta, and T. Yoshinaga, 'Design of Producer-Order Parallel Queue Processor Architecture", Proc. of International Workshop on Modern Science and Technology (IWMST 2004), September 2-3, 2004.

94. M. Akanda, A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "High performance Hybrid Processor Architecture with Efficient Hardware Usability", Proc. of International workshop on Modern Science and Technology (IWMST 2004), September 2-3, 2004.
95. H. Sasaki,Y. Okumura, A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "Theoretical Evaluation of Simultaneous Multi threading Parallel Queue Processor Architecture", Proc. International Conference on Circuits/Systems, Computers and Communications, July 2004.
96. Ben Abdallah, M. Arsenji, K. Kiuchi, M. Akanda, S. Shigeta, T. Yoshinaga, and M. Sowa, "PQPpfB: Parallel Queue Processor Architecture in Verilog-HDL", Proc. of 66th Information Processing Society of Japan, pp. 3F-4, March 2004.
97. T. Viet, T. Toshinga, A. Ben Abdallah, and M. Sowa, "Optimization for Hybrid MPI-OpenMP Programs on a Cluster of SMPs", SACSIS 2004.
98. Musfiquzzaman, A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "Queue Computation Mechanism For Parallel Execution in Parallel Queue Processor", Proc. of Information Processing Society of Japan , Vol. 60, pp. 3F-4, 2004. Canedo Arquimedes†, Abderazek Ben, Yoshinaga Tsutomu, Sowa Masahiro, "A General Purpose Assembler for Queue Computers", Proc. of IPSJ Symposium, 2004,[paper.pdf]
99. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "On the Design of a Register Queue Based Processor Architecture (FaRM-rq)", Lecture Note on Computer Scinece LNCS 2745, International Symposium of Parallel and Distributed Processing and Applications (ISPA 2003), pp.248-262, July 2003.
100. L. Q. Wang, A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "QJAVAC: Queue-Java Compiler Design for High Parallelism Queue Java Bytecode", Proc. of International Technical Conference in Circuits/Systems, Computers and Communications (ITC-CSCC2003), pp. 900-903, July 2003.
101. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "Architectural Issues in the Design of a High Performance Parallel Queue Processor", Proc. of 4th Tunisia-Japan Symposium on Science and Technology (TJASSST2003), April 2003.
102. Tao. Q. Viet, T. Yoshinaga, A. Ben Abdallah, and M. Sowa, "A Hybrid MPI-OpenMP Solution for a Linear System on a Cluster of SMPP", SACSIS03, pp.299-306, 2003.
103. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "A Reduced Bit-Width Instruction Set Architecture for Q-mode Execution in Hybrid Processor Architecture (FaRM-rq)", Proc. of Information Processing Society of Japan, pp. 19-23, June 2003.
104. L. Wang, A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "Fast, Effective Instruction Generation Algorithm For Queue-Java Compiler (QJAVAC)", Proc. of Information Processing Society of Japan, Vol.2003, No.40, pp.55-60, 2003.
105. L. Wang, A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "An Ambiguous Context-Free Grammar for Deterministic Parsing In Queue-Java Compiler", Proc. of Information Processing Society of Japan, Vol.2003, No.62, pp.7-12, 2003.
106. L. Wang, A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "QJAVAC: Queue-Java Compiler Design for High Parallelism Queue Java", Proc. of IEICE Technical conference, 2003.
107. T. Q. Viet, T. Yoshinaga, A. Ben Abdallah, and M. Sowa, "A Hybrid MPI-OpenMP Solution for a Linear System on a Cluster of SMPs", Proc. of Symposium on Advanced Computing Systems and Infrastructures, pp.299-306, 2003.
108. Ben Abdallah, "Dynamic Instructions Issue Algorithm and a Queue Execution Model Toward the Design of Hybrid Processor Architecture", Ph.D. thesis, Graduate School of Information Systems, the Univ. of Electro-Communications at Tokyo, March 2002.
109. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "Complexity Analysis of a Functional Assignment Register Microprocessor", Proc. of the Int. Workshop on Modern Science and Technology (IWMST02), pp.116-123, Sep. 2002.
110. Ben Abdallah, K. Nikolova, and M. Sowa, "FARM-Queue Mode: On a Practical Queue Execution Model", Proc. of the Int. Conf. on Circuits and Systems, Computers and Communications, pp.939-944, July 2001.
111. Kiriuka Nikolova, A. Ben Abdallah, and M. Sowa, "Dynamical Critical Path Parallelism-Independent Scheduling Algorithm for Distributed Computing Systems", Proc. of the International Technical Conference on Circuits and Systems, Computers and Communications, pp. 929-934, July 2001.

112. M Sowa, BA Abderazek, S Shigeta, K Nikolova, T Yoshinaga, "Proposal and Design of a Parallel Queue Processor Architecture (PQP)", Prof. of the Int. Conference on Parallel and Distributed Computing and Systems ((PDCS 2002), pp.549-554, 2002.
113. Ben Abdallah, K. Nikolova T. Yoshinaga, and M. Sowa, "FARM QUEUE MODE: On a Practical Queue Execution Model (QEM)", Tunisia-Japan Workshop on Science and Socity (TIWSS'01), October 2001.
114. Ben Abdallah, Mudar Sarem, and M. Sowa, Dynamic Fast Issue Mechanism (DFI) for Dynamic Scheduled Processors, IEICE transactions on Fundamental of Electronics, Communications and computer Science, Vol. E83-A No.12 pp.2417-2425, Dec. 2000.
115. Ben Abdallah, K. Nikolova, and M. Sowa, "FARM-Queue Execution Model: Towards an Alternative Computing Paradigm", Proc. of IPSJ Symposium, Yokohama pp.99-100, March 2000.
116. Ben Abdallah, M. Sarem., and M. Sowa, "Acyclic DFG on a Queue Machine", Proc. of IPSJ , Tokyo, pp.119-120, 2000.
117. Ben Abdallah, and M. Sarem., "Instruction Scheduling System for Super scalar Processor", Prof. of JSPP2000, Tokyo, pp.161, Apr. 2000 .
118. Ben Abdallah, Mudar Sarem, and M. Sowa, "Dynamic Fast Issue Mechanism (DFI) for Dynamic Scheduled Processors", IEICE transactions on Fundamental of Electronics, Communications and computer Science, Vol. E83-A No.12 pp.2417-2425, Dec. 2000.
119. Ben Abdallah, and M. Sowa,"Write-Once Algorithm to Boost Performance in a Resource Shared Superscalar Processors (RSSP)", 3rd Tunisian Interdisciplinary Workshop on Science and Society, 2000.
120. Ben Abdallah, and M. Sowa, "DRA: Dynamic Register Allocator Mechanism for FaRM Microprocessor", Proc. of the 3rd International Workshop on Advanced Parallel Processing Technologies (APPT'99), pp.131-136, October 1999.