Research on Adaptive Computing

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Abstract

ASL focuses on research and education of new methodologies and novel architectures for current and emerging technologies, and microelectronic devices. These devices form the core technology for communications and personal computing, industry, business, defense, etc. For such devices, there is a need for efficient error detection, diagnosis and recovery protocols. There is also a need for architectures that can combine fault tolerance aspects with performance aspects in an adaptive manner, adapting to different runtime environments and different user requirements. For these goals, we explore adaptive hardware configurations, novel low-power design methodologies and architectures, and adaptive algorithms for the design of a reliable systems. Our recent research projects include self-adaptive microprocessor, architecture design for robust system resilient to permanent and transient faults, and Highly-reliable Intra- and Inter-Chip Network-on-Chip for future Many-core Systems.

Highly-reliable Intra- and Inter-Chip Interconnection Networks

PHENIC: Silicon-Photonics Network-on-Chip for Low-power, High-throughput Many-core Systems

The huge computing power of many-core multi-processor systems will require very large on-chip and off-chip data transfer rates (> 100TB/s). One efficient technology for transmitting this level of information is the optical interconnects, which promise significant advantages over their electronic counterparts. In particular, optical on-chip interconnect (ONoC)) offers a potentially disruptive technology solution with fundamentally low power dissipation that remains independent of capacity while providing ultra-high throughput and minimal access latency. In addition, when combined with 3D integration technology, ONoC offers advantages over 2D NoC design, such as shorter wire length, higher packing density, and smaller footprint [1,2,3,4,5].

Our ASL team will build a sophisticated hybrid electronic-photonic interconnect layer including microsources, photodetectors and different advanced wavelength routing functions. We will demonstrate the application of such electornic-photonic ICs in on-chip optical network. Our approach which inherits several promising features from our earlier proposed OASIS 3D-NoC, offers low-latency data propagation and ultra-wide bandwidth by leveraging wavelength-division multiplexing (WDM) and time-division multiplexing (TDM). The final goal is is to provide a compact, low-power-consumption, high bandwidth and low-latency photonic on-chip interconnection network with full CMOS-compatibility.

OASIS: Scalable Packet-Switched Network-on-Chip Architecture for Multicore Systems

Future System-on-Chip (SoC) will contain hundreds of components made of processor cores, DSPs, memory, accelerators, and I/O all integrated in a single die area of just a few square millimeters. Such small and complex SoC will be interconnected via a novel on-chip interconnect closer to a sophisticated network than to current bus-based solutions.

This network must provide high throughput and low latency while keeping area and power consumption low. Our research effort is about solving several design challenges to enable such new NoC paradigm in many-core systems. In particular, we are investigating implementation techniques for basic building blocks, new topologies, flow control techniques, and low-latency, high-throughput/fault-tolerant routing algorithms [1-24]

Adaptive System Design and Manycore SoC Design for Real-time Bio-medical and Vision-based Object Localization and Recognition Applications

Many ubiquitous applications, such as bio-medical, vision-based object localization and recognition or ADAS applications, are characterized by complex and data-intensive computations which complicate the task of achieving real-time performance on today's technology. Power efficiency is also a real challenge if these applications are run on battery powered mobile systems. Since there is no single architecture that is capable of fulfilling all these requirements, such systems require some kind of adaptivity. This means systems should monitor themselves, analyze their own behavior, and adapt to several execution environments.

The goal of this research, which combines the developed algorithms and techniques from our other two topics, is to research and develop new algorithms and techniques for a power-efficient and real-time system which exploits (whenever possible) all kinds of parallelism (ILP, DLP, TLP and multicore). Our target is computation intensive applications, such bio-medical and object-recognition applications. This includes coordinated tasks on all system components ranging from core level architecture, to compiler and runtime systems, all the way to hardware techniques. Such an approach naturally requires bidirectional data flow and information exchange between components, and therefore new set of dynamic interfaces between the individual components, as well as adaptivity within each module [21,15,7].

BANSMOM: Real-Time Multicore System for Remote Monitoring of Elderly Health

OASIS-VP: Research and Development of Vision Processor

With the advance in microprocessor technology, demands for practical vision and image recognition applications have been appearing in automobile, security, surveillance, and robot applications. Processing multi-objects recognition require higher computing power, making it difficult to perform the computation on conventional shared bus general-purpose processors, despite the recent dramatic improvements in processor performance. Therefore, specialized architecture for communication and computation are needed for high-performance image recognition tasks. Three dimensional Networks-on-Chip (3D-NoC) has been proposed as a promising architecture which combines the high parallelism of Network-on-Chip (NoC) interconnect paradigm with the high-performance and lower interconnect-power of 3-dimensional integration circuits. However, as 3D-NoCs keep showing their advantages against 2D-NoC architectures, their reliability is put under question

The main goal of this project is to research about algorithms and, architecture for a high-performance vision processor. The system is based on our earlier developed reliable Network-on-Chip (OASIS). We will first research about efficient algorithm for recognition of multi-objects in real-time. Then, we will perform research about novel architecture which can effectively detect, diagnosis, and recover from large number of transient faults

in the proposed vision processor. This study should cover all the system components that are most susceptible to failure such as inter-router links, input-buffer, and the crossbar. At the end of this research, the final design should be implemented on a real chip.

SEA: Self-Adaptive Processor

This research is about a novel computing model and architecture based on an innovative self-adaptation behavior, which will provide scalability, high resource utilization, and high-performance by dynamically synthesizing the right resources composition based on temporal program performance demand(s). A given program is considered as a set of small objects competing with other programs running on the same many-core platform. In this computing model, a given program can dynamically occupy/find new space and spread/migrate its computation (various parallelism levels) to appropriate neighbour cores. Using our dynamic temporal-allocation-technique, a given program can de-allocate resources according to its new performance requirement [51].

Architecture and Micro-architecture of Low-power, High-performance Microprocessors

Research on Energy-aware Scheduling and Resource Allocation in Cloud Computing Systems

A cloud computing system is essentially a large-scale distributed computing system consisting of large heterogeneous hardware and software resources (components). Cloud computing is characterized by its scalable resource allocation for various applications/Workloads. This characteristic can be realized by virtualization technologies with many-core processors. We are investigatigating the problem of energy-aware scheduling and resource allocation schemes for different workloads exploiting power consumption characteristics of heterogeneous many-core processors.

Low-power High-performance Queue Computer

Future systems will expose a huge amount of parallelism requiring +1000 cores. As a result, current programming models and applications cannot be used to exploit these terascale systems. Our aim in this research is to propose a complete solution that can exploit the terascale parallelism efficiently. We are researching in both hardware and software sides. In the software side, we are focusing on the programming model, compiler optimizations. On the hardware side, we are focusing on a scalable architecture using available execution cores and interconnection networks. Our previous work on Data-flow Queue computing principles are again re-visited in this research and exploited at all levels to overcome the current limitations of traditional control-flow model [34-123].

Reliable Concurrent VLSI@ASL

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