

# SYA14 - Neuromorphic Computing

## *Lab 7*

### 1 Objective

In this lab, we will test and evaluate the DN-SoC: an SoC of Neuromorphic Computing

### 2 Prerequisite

The following are the prerequisites of this exercise:

- Verilog HDL
- FPGA

### 3 Ex 7.1: The SoC

Please download the source code from: [https://web-ext.u-aizu.ac.jp/misc/neuro-eng/book/NeuromorphicComputing/lab/DN-SoC\\_main.zip](https://web-ext.u-aizu.ac.jp/misc/neuro-eng/book/NeuromorphicComputing/lab/DN-SoC_main.zip)

Please follow the README.MD file to know how to run it.

#### 3.1 Exercise content

Run the example source code and report the result.

### 4 Submission format and Deadline

Your report should be prepared in English and should contain the following:

1. Your name, your ID, and the Lab #.
2. All reports
3. Submission format: soft copy.

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Note: This Laboratory is designed for the book <sup>1</sup>

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<sup>1</sup>Book: Neuromorphic Computing Principles and Organization 1st, Edition, ISBN-10: 3030925242, ISBN-13: 978-3030925246, Publisher: Springer, May 2022.