Computer Logical Design Laboratory

Tsuneo Tsukahara
Professor

Robert H. Fujii
Associate Professor

Yukihide Kohira
Assistant Professor

Tsuneo Tsukahara:

- Software-Defined Radio Transceivers

  Related to this topic, the following work was done in 2012.

  A High-Precision Quadrature Modulator and a Spectrum-Analyzing Method for Multi-band Wireless Transceivers:

  Recently the demand for wireless systems such as sensor networks has been rapidly growing. However, radio-wave resources are limited and invaluable especially in these days. Therefore, software-defied radios (SDRs) and cognitive radios, which is a principal application of SDR, can be the key to greatly improving frequency-spectrum efficiency. SDRs demand flexibility and reconfigurability in RF (Radio Frequency) circuits. Therefore, a spectrum-efficient wireless transceiver architecture is indispensable. In this research, we proposed a multi-band wireless transceiver using a high-precision complex quadrature modulator (HP-CQMOD) and a spectrum-analyzing receiver suitable for sensor networks. As the final goal of our research, we would like to establish a reconfigurable wireless communicator, whose frequency band can be changed according to communication conditions and/or a country's regulations using reconfigurable RF and baseband processors and downloadable software. This is a kind of cognitive radios based on SDR (Software-Defined Radios). In recent years, multi-level modulations such as Quadrature Amplitude Modulation (QAM) are or will be used in Wireless LANs, digital TVs, and the 4th-generation cell-phones. So, very small modulation errors of QMOD are strongly demanded. In the 2012, we have concentrated on circuit design of low-power HP-CQMODs and linear power

amplifiers in the transmitter. Moreover, we devised low-distortion receiver front-end circuits and designed digitally-controlled oscillators (DCOs) and time-to-digital converters (TDCs) for all-digital PLLs (ADPLL) for carrier-signal generation.

RF/IF building blocks we designed have three features as follows:

1. Low-power high-precision complex quadrature modulators are newly developed, featuring folded-cascode or passive quadrature mixers.
2. We proposed linear CMOS power amplifiers using compensation techniques for transconductance and capacitance non-linearities.
3. Low-distortion and wideband techniques are devised for RF low-noise amplifiers and mixers.

Yukihide Kohira:

We investigate *design automation methodology for LSI circuits*. Due to the increase of scales of LSI circuits and the decrease of time to market of LSI products, design automation systems are widely used in order to design LSI circuits. Since the performance of LSI depends on the used design automation systems, it is important to develop design automation methodology continuously in order to obtain good products.

Our research interests are design automation for clock synchronous framework and layout design. In 2012, we focused on following three topics.

General-synchronous Framework

In general-synchronous framework, a clock is distributed periodically to all registers but the clock is not necessarily distributed simultaneously. General-synchronous framework is expected to obtain LSI circuits with high performance and low power consumption. The target of this research is to establish a design automation system for general-synchronous framework. In 2012, we investigated clock scheduling in which the number of clock domains is restricted to two to obtain circuits with high performance without increasing power consumption.

Deskew

In resent LSI circuits, process variations increase significantly because of the progress of the process technology. The process variations significantly cause delay variations and delay variations affect the performance and the yield of VLSI chips. If the circuit cannot work at the testing process after the

fabrication of LSI chips, the circuit can be recovered by deskew in which delay of the programmable delay elements is adjusted. The target of this research is to establish a design automation system for deskew which can improve the yield of LSI chips. In 2012, we proposed the delay turning method to improve the yield and confirmed the effectiveness of deskew.

Placement

In the recent LSI design, it is difficult to obtain a placement which satisfies both design constraints and specifications due to the increase of the circuit size, the progress of the manufacturing technology, and the speed-up of the circuit performance. Analytical placement methods are promising to obtain the placement which satisfies both design constraints and specifications. In 2012, we proposed an acceleration method by GPGPU for an analytical placement method.

Refereed Proceeding Papers

[fujii-01:2012] F. Watanabe and R.H. Fujii. Sequence Learning and Generation Using Spiking Neural Network. In Hanoi University of Science, Technology, and University of Technology Sydney, editors, *The fourth International Conference on Communications and Electronics*, pages 500 – 505, Hue, Vietnam, August 2012. IEEE, Korea Information and Communications Society, and Hanoi University of Science and Technology, IEEE.

A neural network that uses supervised learning is proposed for generating a desired spike output sequence in response to a given input spike sequence.

Unrefereed Papers

[kohira-01:2012] H. Mashiko and Y. Kohira. A Delay Tuning Method of Programmable Delay Element with Two Delay Values for Yield Improvement. In *IEICE Technical Report (VLD2012-69)*, volume 112, pages 57–62, November 2012.

[kohira-02:2012] Y. Kohira and A. Takahashi. An Optimum 2-Clustering Method in General-Synchronous Framework. In *The 25th Workshop on Circuits and Systems*, pages 178–183, July 2012.

[kohira-03:2012] Y. Kohira and Y. Takashima. An Acceleration Method by GPGPU for Analytical Placement using Quasi-Newton Method. In *IEICE Technical Report (VLD2012-74)*, volume 112, pages 87–92, November 2012.

[tsuka-01:2012] Y. Sato and T. Tsukahara. Linear CMOS PA using Compensation Techniques for Transconductance and Capacitance Non-Linearities. In *The 2012 IEICE Society Conference*. IEICE, September 2012.

[tsuka-02:2012] H. Takahashi and T. Tsukahara. Low-Voltage High-Precision Complex Quadrature Modulator. In *The 2012 IEICE Society Conference*. IEICE, September 2012.

[tsuka-03:2012] T. Ito H. Ito and T. Tsukahara. Gm-based Time Difference Amplifier. In *IEICE Technical Report on Silicon Analog RF Technologies*. IEICE, December 2012.

[tsuka-04:2012] Y. Sato and T. Tsukahara. High Linear Low Noise Amplifier using Compensation Techniques for 2nd and 3rd Distortion. In *IEICE Technical Report on Silicon Analog RF Technologies*. IEICE, 2012.

[tsuka-05:2012] H. Takahashi and T. Tsukahara. Design of a Low-Voltage Operation High-Precision Complex Quadrature Modulator. In *The Papers of Technical Meeting on Electronic Circuits, IEEJ*. IEE Japan, 2013.

[tsuka-06:2012] H. Takahashi and T. Tsukahara. Wide-band Low-Voltage High-Precision Complex Quadrature Modulator. In *IEICE Technical Report on Silicon Analog RF Technologies*. IEICE, December 2012.

Grants

[tsuka-07:2012] T. Tsukahara. Grants-in aid for Scientific Research (KAKENHI C) from JSPS, 2011-2013.

[tsuka-08:2012] T. Tsukahara. Cooperative Research Fund from ADVANTEST, 2012.

Academic Activities

[kohira-04:2012] Y. Kohira, September 2012.

Registration Co-Chair, The 6th IEEE Symposium on Embedded Multicore SoCs.

[kohira-05:2012] Y. Kohira, July 2012.

Program Committee Member, 25th Workshop on Circuits and Systems.

[tsuka-09:2012] T. Tsukahara, 2012.

Member of the IEICE Electronics Society Technical Committee on Integrated Circuits and Devices

[tsuka-10:2012] T. Tsukahara, December 2012.

Hosted the IEICE Silicon Analog RF Workshop at UoA on Dec. 13-14, 2012.

Ph.D and Others Theses

[fujii-02:2012] Taiki Konno. Master's Thesis: Aircraft Auto-pilot Simulation, University of Aizu, 2012.

Thesis Advisor: R. H. Fujii

[fujii-03:2012] Mayumi Irifune. Master's Thesis: Controlling the Phase Difference of Two Coupled Oscillators Using Phase Equation Model, University of Aizu, 2012.

Thesis Advisor: R. H. Fujii

[fujii-04:2012] Yusuke Suzuki. Graduation Thesis: Equipment Control for Three Dimensions, University of Aizu, 2012.

Thesis Advisor: R. H. Fujii

[fujii-05:2012] Ryosuke Torieda. Graduation Thesis: Quadrocopter Simulator, University of Aizu, 2012.

Thesis Advisor: R. H. Fujii

[fujii-06:2012] Naoya Kuriwakai. Graduation Thesis: Neural Network Based P Control of a Mass-Spring System, University of Aizu, 2012.

Thesis Advisor: R. H. Fujii

[fujii-07:2012] Seishu Itabashi. Graduation Thesis: PID Controller Optimization Based on Iterative Physical Experiments, University of Aizu, 2012.

Thesis Advisor: R. H. Fujii

[kohira-06:2012] Koji Yamazaki. Graduation Thesis: A Study of Longest Path Problem for a Differential Pair Net, University of Aizu, March 2013.

Thesis Advisor: Y. Kohira

[kohira-07:2012] Yoshiyuki Kume. Graduation Thesis: Peak Power Reduction using 2-Clustering Method in General-Synchronous Framework, University of Aizu, March 2013.

Thesis Advisor: Y. Kohira

[kohira-08:2012] Junki Kawaguchi. Graduation Thesis: Technology Mapping for Low Power Consumption in General-Synchronous Framework, University of Aizu, March 2013.

Thesis Advisor: Y. Kohira

[tsuka-11:2012] Tomoko Nishiuchi. Graduation thesis, School of Computer Science and Engineering, 2013.

Research adviser: T. Tsukahara

[tsuka-12:2012] Yuya Maeda. Master thesis, Graduate School of Computer Science and Engineering, 2013.

Research adviser: T. Tsukahara

[tsuka-13:2012] Jeewaka Dharmapriya. Graduation thesis, School of Computer Science and Engineering, 2013.

Research adviser: T. Tsukahara