Adaptive Systems Laboratory

Kenichi Kuroda
Professor

Junji Kitamichi
Associate Professor

Ben Abdallah Abderazek
Associate Professor

Yuichi Okuyama
Assistant Professor

037 適応システム学講座

Registered Data: Contents Register? The academic area of this laboratory mainly covers computer design methodology. Reconfigurable computing, formal verification, network on a chip, and educational course design for VLSI are the major themes of this lab.

Short history of the Lab.:

"Computer Education Lab." started in 1993.
1993-1998 Prof. A. Taubin
2000- Prof. K. Kuroda
2002- Prof. J. Kitamichi joined.
2005- Prof. Y. Okuyama joined.
2007- Prof. A. Ben joined.
2008- The title of the laboratory changed to "Adaptive Systems Lab.".

Members of our laboratory are four professors, 1 doctor program student, 8 master program students, and 8(B4)+4(B3) graduate thesis students.

Education:

We have been developing an education program of VLSI design based on VDEC (VLSI Design and Education Center) support. VDEC offers various kinds of design tools without license costs and accepts chip fabrication orders in low price. This program was started as a joint research with Prof. Shima, who left from this university in 2004, in Computer Architecture Laboratory in 2001. Web-based manuals for HDL design, verification, and layout tools have been developed and are being updated depending on VDEC support tools every year. Colaborating with

Computer Organization Lab. and Logic Circuit Design Lab., we are establishing educational materials on embedded systems and FPGA-based design courseware.

Research: Recently, we are now focusing on the higher level design circumstances, such as UML, SystemC, and other HDLs. We developed a new design flow from SFL (one of the HDLs) to SystemC for improving the design efficiency. As to the VDEC-based synchronous circuit technology, various applications such as bio-informatics and network security have been surveyed.

We started a new approach to high performance computing systems with reconfigurable devices collaborating with the RIKEN research group, the PROGRAPE Project. The target of this project is "Desktop Supercomputing System". "Desktop" means low-cost with commercially available FPGAs and PCs. We have been developing interface circuits and new applications such as fluid dynamics, data mining, and others. In collaboration with Prof. S. Sedukhin (Distr. Parallel Proc. Lab.), we have been developing a prototype of RapidMarix Processor System, which is a kind of torus array system specified for high performance matrix operation.

We also started a new approach to high performance computer architecture, "Queue Processor" and Network-on-Chip Architecure based on Prof. Ben's research background.

Members of the Computer Education Laboratory

Prof. Kenichi Kuroda:

Before his coming to this university, he belonged to the NTT laboratories and he was engaged with the research on superconductor devices, SAW devices, and X-ray optics. He joined this university mid 1995. He received his Dr. Eng. from Tokyo University in 1991. After coming to this university, he had been a member of the Computer Device Lab. for 5 years and moved to Computer Education lab. in summer 2000. The lab name changed to "Adaptive systems Laboratory" in 2008. He was interested in VLSI design technology. Especially, reconfigurable device systems are the current major research direction.

Prof. Junji Kitamichi:

He received the B.S. and Ph.D degrees in information and computer sciences from Osaka University, Japan, in 1988 and 1999, respectively. In 1991, he joined the Department of Information and Computer Sciences at Osaka University, Japan, as a research associate. From 1999 to 2002, he was with Cybermedia Center at

Osaka University, where he was assistant professor. In 2002, he joined School of Computer Science and Engineering, the University of Aizu, Japan. His research interests include formal methods for VLSI design, dynamically reconfigurable systems, heuristics and parallel algorithms for combinatorial optmization problems.

Prof. Abderazek Ben Abdallah:

He received his BTS degree from Sfax University in 1990. The BE, ME degrees from HUST Univ. in 1994 and 1997 respectively. In 2002, he received his Ph.D. degree from the Univ. of Electro-communications. From 2002 to 2007, he was a research associate at the Univ. of Electro-communications, Graduate School of Information Systems, then Assistant Professor at the network computing laboratory. He joined the Univ. of Aizu in 2007. His research interests span the areas of computer systems, embedded systems, and VLSI.

Prof. Yuichi Okuyama:

He was born in 1975. He received the M.S and Ph.D degrees in computer science and engneering from the University of Aizu in 1999 and 2002, respectively. He entered NTT Network Innovation Laboratories and was engaged with the development of PCA (Plastic Cell Architecture) devices. He joined the University of Aizu in 2005 as an assistant professor. His current interests are implementation of applications on hardware, tool development for design automation on reconfigurable device(FPGA and other devices) and design of hardware for scientific calculations.

Students :

Doctor Program:

D1: Akram Ben Ahmed..

Master Program:

M2:Yumiko Kimezawa, Yukihiro Kotani, Shuta Yamamoto, Ben A. Achraf.

M1:Ryosuke Kaji, Yoshiaki Kondo, Toshihiro sato, Yoshuke Haraguchi.

Graduation Thesis Students:

B4:Kazuji Kobayashi, Toshiichi Idonuma, Takaaki Ouchi, Yuya Otsuka, Makoto Yoshizawa, Toru Hasegawa, Shu Endo, Tokimasa Shirai

B3:Nakamura Mitsuhiro, Hashimoto Shoji, Baba Shunshuke, Ito Shomu

Edit for TeX Run compile TeX Show PDF TeX compile log

会津大学

Refereed Journal Papers

[benab-01:2012] Akram Ben Ahmed and Abderazek. Ben Abdallah. Architecture and Design of High-throughput, Low-latency and Fault Tolerant Routing Algorithm for 3D-Network-on-Chip. *Supercomputing*, none(http://link.springer.com/article/10.1007nk.springer.com/article/10.1007 2013.

Abstract: Despite the higher scalability and parallelism integration offered by Network-on-Chip (NoC) over the traditional shared-bus based systems, it is still not an ideal solution for future large-scale Systems-on-Chip (SoCs), due to limitations such as high power consumption, high-cost communication, and low throughput. Recently, extending 2D-NoC to the third dimension (3D-NoC) has been proposed to deal with these problems; however, 3D-NoC systems are exposed to a variety of manufacturing and design factors making them vulnerable to different faults that cause corrupted message transfer or even catastrophic system failures. Therefore, a 3D-NoC system should be fault tolerant to transient malfunctions or permanent physical damages. In this paper, we propose a low-latency, high-throughput, and fault-tolerant routing algorithm named Look-Ahead-Fault-Tolerant (LAFT). LAFT reduces the communication latency and enhances the system performance while maintaining a reasonable hardware complexity and ensuring fault tolerance. We implemented the proposed algorithm on a real 3D-NoC architecture (3D-OASIS-NoC) and prototyped it on FPGA, then we evaluated its performance over various applications. Evaluation results show that the proposed algorithm efficiently reduces the communication latency that can reach an average of 38 % and 16 %, when compared to conventional XYZ and our early designed Look-Ahead-XYZ routing algorithms, respectively, and enhances the throughput with up to 46 % and 29 %.

[okuyama-01:2012] T. Sato D. Wei M. Sakai, Y. Okuyama. Nonlinear State-Space Projection Based Method to Acquire EEG and ECG Componects Using a Single Electrode. *International Journal of Life Science and Medical Research*, 2(4):96–100, 2012.

In some diagnoses, such as the polysomnography, simultaneous measurement of the electroencephalogram (EEG) and the electrocardiogram (ECG) is often required. It would be more efficient if both the EEG and ECG could be obtained simultaneously by using a single measurement. In this paper, we introduce a nonlinear state-space projection-based technique to extract the EEG and ECG components from an EEG signal measured with a non-cephalic reference (NCR)

that guarantees accurate detection of R waves in the EEG measurement. Evaluation of the method using simulated data showed that the improved normalized power spectrum in alpha, beta (1330 Hz), and theta bands were accurate. In an accrual EEG, measured using the NCR electrode, it was confirmed that the frequency components of the extracted EEG were accurate, and no spikes that could be attributed to the ECG component were observed in the resultant EEG signal.

Refereed Proceeding Papers

[benab-02:2012] S. Miura A. Ben Abdallah Akram Ben Ahmed, T. Ouchi. Run-Time Monitoring Mechanism for Efficient Design of Application-specific NoC Architectures in Multi/Manycore Era. In *IEEE Proc. of the 6th International Workshop on Engineering Parallel and Multicore Systems (ePaMuS2013'), July 2013*, page NA. IEEE, July 2013.

Abstract—One of the major design challenges of Networkon-Chip interconnect is the storage buffers. They occupy a signicant portion of the system ' s area and so they are considered as main " power-hungry " components. Deciding the appropriate buffers size and implementation in these systems is the key technique for increasing system performance and also for reducing overall area and power consumption. However, this goal is very hard to achieve with traditional design approaches, where design decisions of the main architectural parameters are generally made with slow and inaccurate software simulation or theoretical modeling. In order to quickly capture and decide the optimal buffers size and the whole system behavior, we propose in this work an efcient design method for Network-on-Chip architecture based on a novel run-time monitoring mechanism (RMM). The system monitors the trafc ow at different system ' s resources and sends the monitored run-time trafc information to a specialized controller. In addition, our proposed design method allows to easily compute optimal architecture hardware parameters (i.e Buffer size) and allocate the appropriate values on demand to satisfy the requirements of any given application. The RMM mechanism was designed in hardware and integrated into our NoC system (PNoC)1 . From the evaluation results, we conclude that the system performance in terms of execution time was about 27compared with traditional design methods over several benchmark programs

[benab-03:2012] Akram Ben Ahmed, Achraf Ben Ahmed, and A. Ben Abdallah. Akram Ben Ahmed and Achraf Ben Ahmed and A. Ben Abdallah and

Deadlock-Recovery Support for Fault-tolerant Routing Algorithms in 3D-NoC Architectures. In *IEEE Proceedings of the 67h International Symposium on Embedded Multicore SoCs (MCSoC-13)*, page To appear. IEEE, 2013.

Abstract—In this paper, we present a low-cost deadlock recovery technique for fault-tolerant routing algorithms in 3-dimensional Networks-on-Chip (3D-NoC) systems, called Random-Access-Buer (RAB). RAB detects the presence of deadlock in the buer and removes it with no considerable performance drop. The proposed deadlock-recovery technique was implemented on our earlier designed 3D-NoC system (3D-OASIS-NoC1), which adopts Look-Ahead-Fault-Tolerant routing algorithm (LAFT). Evaluation results show that, at low fault-rates, the proposed technique does not affect the performance when compared to the previous system. At high fault-rates, RAB manages to avoid deadlock while the earlier system fails and the communication is blocked. The benets acquired with RAB comes with only small extra hardware illustrated in 7 percent additional area and a slight 3.5 percent power overhead when compared to the previous 3D-OASIS-NoC system.

[benab-04:2012] A. Ben Abdallah Achraf Ben Ahmed. Hardware/Software Prototyping of Dependable Real-Time System for Elderly Health Monitoring. In *IEEE Proc. of the World Congress on Computer and IT, ICMAES, June 2013*, page NA, June 2013.

Abstract—Recent technological advances in sensors, lowpower microelectronics, and wireless networking enabled the proliferation of wireless sensor networks for wide applications. One of the promising applications of this domain is the distributed remote health monitoring of elderly people. An effective approach to speed up this and other bio-medical applications is to integrate a very high number of processing elements in a single chip so that the massive scale of negrain parallelism inherent in several bio-medical applications can be exploited efciently. In this work, we present architecture and preliminary prototyping results of a novel dependable real-time system (BANSMOM1) targeted for elderly health monitoring. The proposed system achieves its real-time performance via parallel processing technique and a so called period-peak detection algorithm (PPD) for processing multi-lead Electrocardiography records

[okuyama-02:2012] Junko Tazawa, Yuichi Okuyama, Yuichi Yaguchi, Toshiaki Miyazaki, Ryuichi Oka, and Kenichi Kuroda. Hardware Implementation of Accumulated Value Calculation for Two-Dimensional Continuous Dynamic Programing. In *2012 IEEE 6th International Symposium*

on Embedded Multicore SoCs (MCSoC 2012), page DOI 10.1109/MCSoC.2012.10, Sep 2012.

We propose an efficient hardware accelerator for the calculation of accumulated values of two-dimensional continuous dynamic programming (2DCDP). The 2DCDP is a powerful optimal pixel-matching algorithm between input and reference images which can be applied to image processing, such as image recognition, image search, feature tracking, and 3D reconstruction. However, it requires large computation time due to its time and space complexities of $O(N^4)$. We analyze the computation flow of the 2DCDP algorithm and propose a high- performance architecture for a hardware accelerator. Parallelized accumulated minimum local distance calculators and a toggle memory structure are newly introduced to reduce the computation cost and memory. The proposed architecture is implemented into an FPGA, Stratix IV, EP4SE820. Its maximum operation frequency is 125.71 MHz. The preliminary evaluation reveals that the parallel processing by 32 PEs for the accumulated value calculation for 32x32 input and reference images can be sped up to 77 times at the maximum operation frequency of 100 MHz compared to the processing with a multi-core processor.

Unrefereed Papers

[kitamiti-01:2012] Y. Nishimaki, Junji Kitamichi, and T. Miyazaki. A Simulator Visualizing Inside Behaviors of MIPS Processor. In *Proceedings of the 76th National Convention of IPSJ*, pages 6ZC–7. IPSJ, March 2013.

[kitamiti-02:2012] Yosuke Wakisaka, Naoki Shibata, Junji Kitamich, Keiichi Yasumoto, and Minoru Ito. Task Scheduling for Multi-core Processors Systems Considering Turbo Boost and Hyper Threading. In *IPSJ SIG Technical Reports,Vol.2012-HPC-23,No.136*, pages 1 – 8. IPSJ, October 2013.

In this paper, we design an operating frequency model with Turbo Boost and Hyper-Threading Technology used in recent multi-core processors from actual measurements and propose a task scheduling algorithm considering a network contention and a dynamic frequency shift based on the designed model. When scheduling the task graph to processors, firstly, the proposed algorithm generates the combinational permutation that satisfies the dependence among the tasks. Then, the number of tasks is determined as the input parameter. In

regard to the generated permutations, the proposed algorithm calculates the processing time of a task node under the defined operating frequency considering the processor usage. Then these tasks are scheduled temporarily. This algorithm estimates the processing time of the entire task graph for the temporary scheduling result and selects the best of temporary scheduling results in which the estimated processing time is the shortest. We compared the proposed algorithm and the existing task scheduling algorithms which consider the network contention and do not consider the dynamic shift of the operating frequency with Turbo Boost and Hyper-Threading Technology, the proposed algorithm reduced the total processing time by 16%.

[kitamiti-03:2012] S. Yamamoto and J. Kitamichi. A Heuristic Approach for Channel Assignment Problem using Ant Colony Optimization and Neural Network Algorithm. In *Proceedings of the 76th National COnvention of IPSJ*, pages 1M–3. IPSJ, March 2013.

Recently, demands for cellular radio network are increasing cellular devices such as smart phones or wireless sensor devices. Channel Assignment Problem(CAP) are becoming more important in order to make the most of limited channels. This paper proposes a combined method of Ant Colony Optimization(ACO) and Neural Network Algorithm(NAA) for the CAP. ACO is utilized for explore large solution space and NNA is used for getting into a local optimum solution immediately. The proposed method can achieve similar solution ability in some instances as an existing method, and can acquire 2% smaller interference solution in 3 benchmarks in average and the same interference solutions in 2 benchmarks compared with an existing method. We expect that a larger number of ants and better parameter tuning can achieve better solution using our proposed method.

[kitamiti-04:2012] H. Kotani and J. Kitamichi. An Implementation of Real Time OS for Multi-processor on FPGA. In *Proceedings of the 76th National COnvention of IPSJ*, pages 2L–10. IPSJ, March 2013.

Recently, multi-core processors are featured at the embedded field. On-chip processors have an advantage of the processing performance and power consumption. Compared to general-purpose systems, embedded systems have often dedicated functions. In the field of embedded systems, tightly coupled and functional distributed type multi-processors are often used. OS of multi-core processors is very useful in order to operate efficiently hardware resources of multi-core processor system. On-chip processors are expected to adapt to various embedded systems. In this paper, we prototype various system configura-

tion and develop RTOS that can be used in university education. Therefore, we adopt Field Programmable Gate Array (FPGA) and Nios II processor. And, we develop a RTOS for embedded multi-core processor system and some hardware modules and APIs to improve performance of the proposed RTOS. In addition, we reduce the burden on the designer by unifying setting parameters of RTOS responding to variety of FPGA boards and the burden on the designer by unifying or automatizing description generation of device dependent parameters. We improve the usability of the designer by developing APIs of resetting or getting the value of a register for a timer module. Tasks are able to start without synchronization, and we improve processor performance by reducing idle time at the start. We improve performance by developing a multi-port mutex and a multi-port shared memory. As a result, we automate generation of the configuration of all 24 files in the target device dependent parts and all 64 variable definitions.

[okuyama-03:2012] Kenichi Kuroda Tokimasa Shirai, Yuichi Okuyama. Design of Coarse-grain Processing Element for Matrix Array Processor on FPGA. In *24th IPSJ Tohoku branch workshop*. IPSJ, Feb. 2012.

[okuyama-04:2012] Ryosuke KAJI, Yuichi OKUYAMA, Yuichi YAGUCHI, Kenichi KURODA, and Ryuichi OKA. Proposal and Implementation of Acceleration Methods for Two-dimentional Continuous Dynamic Programming by GPGPU. In *Proc. of 38th PARTHENON Workshop*, pages 37–42. PARTHENON Society, Sep. 2011.

[okuyama-05:2012] Kazuki Kobayasahi, Yuichi Okuyama, and Kenichi Kuroda. Design of High Performance API for Direct Memory Access on Portable PCI Express Interface. In *24th IPSJ Tohoku branch workshop*. IPSJ, Feb 2012.

Books

[benab-05:2012] Abderazek Ben Abdallah. *Multicore Systems-on-Chip: Practical Hardware/Software Design, 2nd Edition*, volume http://www.springer.com/computer/hardware/book/978-94-91216-91-6. Springer, 2nd edition edition, June 2013.

Book Description: -Provides practical hardware/software design techniques for Multicore Systems-on-Chip -Provides a real case study in Multicore Systems-on-

Chip design -Provides interaction between the software and hardware in Multicore Systems-on-Chip -Provides detailed overview of various existing Multicore SoCs System on chips designs have evolved from fairly simple unicore, single memory designs to complex heterogeneous multicore SoC architectures consisting of a large number of IP blocks on the same silicon. To meet high computational demands posed by latest consumer electronic devices, most current systems are based on such paradigm, which represents a real revolution in many aspects in computing. The attraction of multicore processing for power reduction is compelling. By splitting a set of tasks among multiple processor cores, the operating frequency necessary for each core can be reduced, allowing to reduce the voltage on each core. Because dynamic power is proportional to the frequency and to the square of the voltage, we get a big gain, even though we may have more cores running. As more and more cores are integrated into these designs to share the ever increasing processing load, the main challenges lie in efficient memory hierarchy, scalable system interconnect, new programming paradigms, and efficient integration methodology for connecting such heterogeneous cores into a single system capable of leveraging their individual flexibility. Current design methods tend toward mixed HW/SW co-designs targeting multicore systems on-chip for specific applications. To decide on the lowest cost mix of cores, designers must iteratively map the device's functionality to a particular HW/SW partition and target architectures. In addition, to connect the heterogeneous cores, the architecture requires high performance complex communication architectures and efficient communication protocols, such as hierarchical bus, point-to-point connection, or Network-on-Chip. Software development also becomes far more complex due to the difficulties in breaking a single processing task into multiple parts that can be processed separately and then reassembled later. This reflects the fact that certain processor jobs cannot be easily parallelized to run concurrently on multiple processing cores and that load balancing between processing cores especially heterogeneous cores is very difficult.

Grants

[benab-06:2012] A. Ben Abdallah. Distributed Shared-Buffers Network-on-Chip for High-performance Many-core Systems, 2013.

CRF funding, Final Phase, 2013-2014.

Academic Activities

[benab-07:2012] A. Ben Abdallah, 2013.

-Steering Chair and General Co-Chair, 2014 International Conference on High Performance Compilation, Computing and communications (HP3C-2014), Aizu-Wakamatsu, Japan, September 24-26, 2014. -Steering Chair and General Co-Chair, 8th IEEE Symposium on Embedded Multicore Systems-onchip (MCSoC-14), The University of Aizu, Aizu-Wakamatsu, Japan, September 24-26, 2014. -Steering Chair and General Co-Chair, IEEE 7th International Symposium on Embedded Multicore/Manycore SoCs, (MCSoC 2013), National Center of Sciences, Tokyo, Japan, September 26-28, 2013. -Chair, ACM EL Aizu Chapter, 2012- -Steering Chair, IEEE 6th International Symposium on Embedded Multicore SoCs, The University of Aizu, Aizu-Wakamatsu, Japan, September 20-22, 2012. -Program co-chair, 5th International Workshop of Engineering Parallel and Multicore Systems, July 4-6, 2012, Palermo, Italy

[benab-08:2012] A. Ben Abdallah, 2013.

Guest Editor -"Special Issue on Programming and Architecture Support for Embedded Multicore SoC Systems", International Journal of Adaptive and Innovative Systems (IJAIS) , InderScience, 2013; -"Special Issue on Embedded Multicore and Many-core Architectures", International Journal of Embedded Systems (IJES), InderScience, 2013. Joined the Editorial Board of: -Journal of Adaptive and Innovative Systems (IJAIS), 2013- -Journal of Embedded Systems, 2013- Served as Reviewer on the 2013 for: - IEEE Micro - IEEE Network Magazineo IET journal of Circuits, Devices & Systems - Journal of Supercomputing - IET journal of Circuits, Devices & Syste Served as TPC members for: -The 16th International Conference on Network-Based Information Systems (NBiS 2013), September 4-6, 2013, Gwangju, Korea. -6th International Workshop on Engineering Parallel and Multicore Systems,July 3-5, 2013, Taichung, Taiwan -IEEE Symposium on Low-power and High-speed Chips (COOL Chips XI), Yokohama, April 17- 19, 2013. -6th Workshop on Engineering Parallel and Multicore Systems,July 3-5, 2013, Taichung, Taiwan -Computers, Communications and IT Applications Conference (ComComAp 2013, HKUST, Hong Kong,April 1-4, 2013.

[kitamiti-05:2012] Kitamichi J., 2012.

member. IEEE

[kitamiti-06:2012] Kitamichi J., 2012.

member, IPSJ

[kitamiti-07:2012] Kitamichi J., 2012.

member, IEICE

[okuyama-06:2012] Yuichi Okuyama, April 2012.

Steering committee, PARTHENON sosiety 2012.

[okuyama-07:2012] Yuichi Okuyama, April 2012.

Regular member, IEICE 2012.

[okuyama-08:2012] Yuichi Okuyama, April 2012.

Regular member, JSSST 2012.

[okuyama-09:2012] Yuichi Okuyama, April 2012.

Committee member, IEICE CPSY 2012.

Ph.D and Others Theses

[benab-09:2012] A. Ben Abdallah. 1. Takayuki Ochi, "A Quantitative Performance Study of Shared Memory Multicore Systems", "'Bachelor Thesis, School of Computer Science and Engineering,The University of Aizu, Feb. 2013, 2. Shuu Endou, "Hardware Prototyping and Evaluation of Distributed Routing Core Network-Interface for OASIS NoC Architecture", "'Bachelor Thesis, School of Computer Science and Engineering,The University of Aizu, Feb. 2013, 3, Y. Kimezawa,"Towards the Design of Dependable Real-Time System for Remote Health Monitoring of Elderly People", Master's Thesis, Graduate School of Computer Science and Engineering, The University of Aizu, Feb. 2013. 4. Achraf Ben Ahmed, "Interactive Real-time Interface for Smart Remote Health Monitoring and Analysis", Master's Thesis, Graduate School of Computer Science and Engineering, The University of Aizu, Feb. 2013., School of Computer Science and Engineering, March 2013.

2 BS students and 2 MS students graduated.

[okuyama-10:2012] Tokimasa Shirai. Graduation thesis, School of Computer Science and Engineering, 2013.

Thesis Advisor: K. Kuroda

[okuyama-11:2012] Toru Hasegawa. Graduation thesis, School of Computer Science and Engineering, Mar. 2013.

[okuyama-12:2012] Toshiichi Idonuma. Graduation thesis, School of Computer Science and Engineering, Mar. 2013.

Thesis Advisor: K. Kuroda

[okuyama-13:2012] Yuya Otsuka. Graduation thesis, School of Computer Science and Engineering, Mar. 2013.

Thesis Advisor: K. Kuroda

[okuyama-14:2012] Takaaki Ouchi. Graduation thesis, School of Computer Science and Engineering, Mar. 2013.

Thesis Advisor: K. Kuroda

[okuyama-15:2012] Kazuki Kobayashi. Graduation thesis, School of Computer Science and Engineering, Mar. 2013.

Others

[benab-10:2012] A. Ben Abdallah. -Entrance Examination Proctor., 2013.

-Entrance Examination Proctor.