

Computer Organization Laboratory



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The following researches are progressed in Computer Organization Laboratory:

Toshiaki Miyazaki:
has mainly two topics as follows:

- *Die-hard sensor network* is a wireless sensor network that has an autonomous function alternation mechanism among sensor nodes as well as ordinary wireless sensor network capabilities such as automatic network establishment. With this mechanism, we can realized self-organized and maintenance-free sensor network systems. Its applications include surveillance of disaster-hit region, and river and forest monitoring. We are developing not only sensor-node hardware but also protocols equipped to the sensor node.
- *Custom Computing* is a research field to realize a dedicated hardware using programmable logic devices such as FPGAs (Field Programmable Gate Arrays) in order to solve a give problem effectively. We focused on a BLAST accelerator.
 - BLAST accelerator: Basic Local Alignment Search Tool (BLAST) is one of the most popular sequence alignment tools. Sequence alignment is used to extract similar parts of the input protein (or DNA) sequence from protein (or DNA) databases, in order to investigate biological evolution and genomic genealogy. It is a very important and difficult task in bioinformatics. Although BLAST is well tuned to effective sequence alignment, the performance is still not enough to deal with the rapid growing of the databases. BLAST consists of three steps: query words

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and neighborhood word list creation (step 1), word-hit search and un-gapped extension (step 2), and gapped extension (step 3). We are developing a hardware accelerator that performs abovementioned all processing steps of for BLAST.

Hiroshi Saito:

Our research interests are design of asynchronous circuits and its automation. Asynchronous circuits are circuits where circuit components are controlled by pairs of local handshake signals instead of a global clock signal. Because of the absence of a global clock signal, asynchronous circuits are low power and low electromagnetic interference compared to synchronous counter parts which use global clock signals. Our research topics are as follows.

- Synthesis of asynchronous circuits from a behavioral model specified by C language
- Design of low power and low energy asynchronous circuits
- Synthesis of networks-on-chip architecture from a behavioral model such as Mathworks Simulink

Refereed Journal Papers

- [hiroshis-01:2013] N. Hamada, M. Iizuka, and H. Saito. An ASIC Design Support Tool Set for Non-pipelined Asynchronous Circuits with Bundled-Data Implementation. *IEICE Transaction*, E96-C(4):482–491, 2013.

This paper proposes an ASIC design support tool set for non-pipelined asynchronous circuits with bundled-data implementation.

- [miyazaki-01:2013] S. Ishikawa, A. Tanaka, and T. Miyazaki. Accelerating BLAST Algorithm using an FPGA. *IPSJ Journal (In Japanese)*, 55(3):1167–1176, 2014.

Basic Local Alignment Search Tool (BLAST) is one of the most popular sequence alignment tools. BLAST consists of preprocessing, seeding, ungapped extension, gapped extension and traceback process. To accelerate BLAST, many hardware accelerators have been proposed. However, their acceleration target is mainly the gapped extension, and other parts are still realized as software that runs on a host machine. In this paper, we propose an accelerator for BLAST, which realizes all processing parts including the preprocessing and the traceback part as hardware. It could avoid the data transfer bottleneck between software and hardware. We also propose two performance improvement techniques for the gapped extension block. An inexpensive FPGA (field programmable gate array) implementation shows that our hardware accelerator performs 791 times faster than a software BLAST, with reasonable hardware cost. Moreover, by applying the performance improvement techniques, the performance of the accelerator becomes more than 840 times faster than the software BLAST.

- [miyazaki-02:2013] Y. Nishimaki, J. Kitamichi, and T. Miyazaki. Development of Education-purpose MISP Processor Simulator System Visualizing Internal Operation Behavior. *IEICE Transactions on Information and Systems (Japanese Edition)*, J96-D(10):2130–2138, 2013.

This paper proposes a processor simulator expected to be used in lectures and/or excises, which are aimed at teaching computer architecture. The target of the simulator is beginners who have basic knowledge and skill to develop simple software programs, but not have deep hardware knowledge. Historically, many processor simulators have been proposed, but they only support the instruction-level simulation. Thus, it is hard

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for the beginners to understand hardware parallelism and how each instruction is executed in a processor, even if they use the simulators. The proposed processor simulator can simulate several variations of MIPS processor architecture, and visualize their internal behaviors using some windows showing different aspects of the instruction execution. The evaluation results using some students show that the proposed simulator is useful for the beginners, compared to other methods for teaching computer architecture.

Refereed Proceeding Papers

- [hiroshis-02:2013] M. Iizuka and H. Saito. A floorplan method for ASIC designs of asynchronous circuits with bundled-data implementation. In *Proc. IEEE International New Circuits and Systems Conference*, pages 1–4, 2013.

This study proposes a floorplan method for asynchronous circuits with bundled-data implementation to support ASIC designs.

- [hiroshis-03:2013] H. Saito H. Katabami and T. Yoneda. Design of a GALS-NoC using Soft-cores on FPGAs. In *Proc. IEEE International Symposium on Embedded Multicore SoCs*, pages 31–36, 2013.

In this paper, we propose a Globally-Asynchronous Locally-Synchronous Network-on-Chip (GALS-NoC) architecture for FPGAs.

- [miyazaki-03:2013] P. Li, S. Guo, T. Miyazaki, and V. Leung. Joint Optimization of Transmission Scheduling and Relay Assignment for Cooperative Communications. In *Proc. IEEE ICC'13*, pages 4638–6342, DOI:10.1109/ICC.2013.6655623, June 2013.

Cooperative communication (CC) has been proposed to increase the wireless channel capacity and reliability by employing multiple single-antenna nodes to form a virtual antenna array. Many efforts focus on exploiting the benefits of CC among multiple source-destination pairs with an unrealistic assumption that each of them communicates over a dedicated channel without interference. In this paper, we investigate the transmission scheduling problem for multiple source-destination pairs under the assistance of a set of dedicated relay nodes on a single channel. By applying the protocol interference model, we propose a concept of cooperative link to characterize the interference regions of CC. Due

to the NP-completeness of optimal scheduling, LP (linear programming) based heuristic algorithms are proposed to maximize the minimum transmission rate under a given relay assignment. Then, without specifying a relay node for each source-destination pair, we study the max-min rate problem by jointly considering transmission scheduling and relay assignment. Heuristic algorithms are proposed to solve this more challenging problem. Finally, extensive simulations are conducted to show that the proposed algorithm outperforms direct transmission substantially.

- [miyazaki-04:2013] T. Miyazaki, S. Yamaguchi, K. Kobayashi, J. Kitamichi, S. Guo, T. Tsukahara, and T. Hayashi. A Software Defined Wireless Sensor Network. In *Proc. IEEE International Conference on Computing, Networking and Communications (ICNC2014)*, pages 847–652, Feb. 2014.

We propose a software-defined wireless sensor network system whose behavior can be redefined even after deployment by the injection of sensor node roles by means of wireless network communications. Two main technologies are used to develop this system, role generation and delivery mechanism, and a reconfigurable wireless sensor network with many reconfigurable sensor nodes. In the role generation and delivery mechanism, a scenario compiler generates roles for sensor nodes based on a user-defined scenario description and then delivers the roles to appropriate nodes. We also propose a reconfigurable sensor node composed of an ultra-low power field programmable gate array (FPGA) and a microcontroller unit (MCU) for altering network behavior. By assigning heavy tasks such as sensor and data processing to the FPGA, overloading of the MCU can be avoided. Using wireless communication, both configuration data for the FPGA and programs to run on the MCU can be injected as roles from outside of the sensor node, enabling easy alteration of sensor node functionality depending on situation and/or application. After introduction of a system overview, a prototype system is described and some experimental results are discussed.

- [miyazaki-05:2013] T. Miyazaki, H. Iwata, K. Kobayashi, S. Yamaguchi, D. Zeng, S. Guo, J. Kitamichi, T. Hayashi, and T. Tsukahara. DASN: Demand-addressable Sensor Network for Active Information Acquisition. In *Proc. ACM the 8th International Conference on Ubiquitous Information Management and Communica-*

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tion (IMCOM2014), page DOI:10.1145/2557977.2557995, Jan. 2014.

In this paper, we propose a new type of sensor network called the demand-addressable sensor network (DASN). DASN actively gets desired information by delivering or addressing users' demands to appropriate places that are expected to have the information. This is in contrast to conventional sensor networks, which simply send sensed data to users. DASN is useful for finding desired information in a short amount of time from a large amount of sensed data generated by a large-scale sensor network. DASN is constructed with a demand-addressable network that integrates many reconfigurable wireless sensor networks and other existing systems. In addition to the demand-addressing mechanism, the demand-addressable network has an in-network data mashup mechanism. The mashed-up data are displayed on the user terminal without any need to install a dedicated application program. It can also mashup useful information acquired from systems already existing in the network without modifying each system. The functions of the reconfigurable wireless sensor network can be dynamically customized by injecting roles specified by the user. Thus, the user can actively get desired information by customizing the sensor network function. The main target of DASN is wide-area disaster site monitoring—for which the DASN features outlined above are suitable. In this paper, we present the concept underlying DASN, its architecture, and current status of development. We also present preliminary experimental results. (Best Paper Award)

[miyazaki-06:2013] Zeng D, Miyazaki T, S. Guo, T. Tsukahara, J. Kitamichi, and T. Hayashi. Evolution of Software-Defined Sensor Networks. In *Proc. IEEE 9th International Conference on Mobile Ad-hoc and Sensor Networks (MSN 2013)*, pages 410–413, DOI:10.1109/MSN.2013.60, Dec. 2013.

After a decade of extensive research on application-specific wireless sensor networks (WSNs), the recent development of information and communication technologies make it practical to realize new WSNs paradigm known as software-defined sensor networks (SDSNs). SDSNs are able to adapt to various application requirements and to fully explore the communication, computation and sensing resources of WSNs. Sensor nodes in SDSNs can be dynamically reprogrammed for different sensing tasks via the over-the-air-programming technique. In this pa-

per, we introduce the concept of SDSNs and outline several pioneering related work and enabling technologies for the realization of SDSNs.

- [miyazaki-07:2013] S. Yamaguchi, T. Miyazaki, J. Kitamichi, S. Guo, T. Tsukahara, and T. Hayashi. Programmable Wireless Sensor Node Featuring Low-power FPGA and Microcontroller. In *The 6th IEEE International Conference on Ubi-Media Computing (UMEDIA2013)*, pages 596–601, DOI:10.1109/ICAwST.2013.6765509, Nov. 2013.

A sensor node often uses a low-performance microcontroller unit (MCU) to reduce its power consumption. However, it is difficult to handle heavy tasks with the MCU. To solve this problem, we developed a new sensor node that uses an ultra-low power field-programmable gate array (FPGA) in addition to an MCU. By assigning heavy tasks, such as sensor and data processing, to the FPGA, we can avoid overloading the MCU. Both the configuration data for the FPGA and the programs running on the MCU can be injected from outside the sensor node using wireless communication. Thus, the functionality of the sensor node can be easily changed depending on the situation and/or the applications.

- [miyazaki-08:2013] H. Huang, D. Zeng, S. Guo, H. Yao, and T. Miyazaki. Stochastic analysis on epidemic dissemination of lifetime-controlled messages in DTNs. In *Proc. The 9th IEEE International Wireless Communications and Mobile Computing Conference (IWCMC 2013)*, pages 1578–1583, July 2013.

To understand the delivery performance of message dissemination in Disruption Tolerant Networks (DTNs), various methods have been proposed in the literature. However, existing work shares a common simplification that the pairwise meeting rate between any two mobile nodes is exponentially distributed. In this paper, instead of relying on such assumption, we jointly consider the transmission range and Random Direction Mobility (RDM) model to stochastically analyze delivery performance of epidemic routing in terms of percolation ratio and delivery delay. Furthermore, we study a controlled epidemic routing, in which any message stays at a mobile node longer than a predefined lifetime should be removed from the node. It can be considered as an age-structure process described by the Susceptible-Infectious-Recovered (SIR) model. To the best of our knowledge, we are the first to characterize the message propagation process by applying the Delay Differential

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Equations (DDEs) in DTNs. The correctness of our analysis is validated by extensive simulations.

- [miyazaki-09:2013] T. Hayashi, H. Fukuhara, Y. Abe, M. Hisada, J. Yamazaki, H. Tokura, T. Miyazaki, and J. Iwase. Joint Optimization of Transmission Scheduling and Relay Assignment for Cooperative Communications. In *Proc. The 15th Asia-Pacific Network Operation and Management Symposium (APNOMS2013)*, pages 1–3, Sept. 2013.

The present paper introduces an intelligent infrastructure for social networking services using a messaging network. The proposed messaging network can provide content/topic-based routing and filtering. The proposed scheme provides a network-centric approach to ensure flexible information aggregation and message mediation for social networking services.

Unrefereed Papers

- [hiroshis-04:2013] K. Takizawa and H. Saito. FPGA を対象とした束データ方式による非同期式回路の設計支援ツールセット. In *VLD2013-SLDM-163*, pages 69–74, 2013.
- [hiroshis-05:2013] S. Miyasono and H. Saito. シングルコア向けのコードを NoC に実装するためのコード分割ツールの検討. In *VLD2013-SLDM-163*, pages 113–118, 2013.
- [hiroshis-06:2013] S. Iwasaki and H. Saito. サイクルタイム制約を考慮した低消費電力な束データ方式による非同期式 AVR プロセッサの設計. In *VLD2013-SLDM-163*, pages 153–158, 2013.
- [miyazaki-10:2013] K Kobayashi and T. Miyazaki. Role Assignment Method for Wireless Sensor Network Based on Scenario Description. In *IPSSJ 76th National Convention*, volume 6W-3, March 2014.
- The student encouragement award
- [miyazaki-11:2013] D. Baba, D. Zeng, and T. Miyazaki. Emulation Environment for a Large-scale Sensor Network. In *IPSSJ 76th National Convention*, volume 6W-4, March 2014.
- [miyazaki-12:2013] S. Yamaguchi and T. Miyazaki. An approach to Sensor Data Processing Using Low-power FPGA in a Wireless Sensor

Node. In *IPSSJ 76th National Convention*, volume 6W-5, March 2014.

[miyazaki-13:2013] N. Suematsu, H. Iwata, and T. Miyazaki. Implementation of Customizable Visual Simulator for MIPS Processor. In *IPSSJ 76th National Convention*, volume 6W-8, March 2014.

[miyazaki-14:2013] S. Ito, D. Zeng, and T. Miyazaki. Comparisons of Database Systems Suitable for Large-scale Sensor Networks. In *IPSSJ 76th National Convention*, volume 3X-1, March 2014.

The student encouragement award

[miyazaki-15:2013] T. Kawasaki and T. Miyazaki. Attribute-based Software Distribution for Wireless Sensor Nodes,. In *IEEE student session in 2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers, Japan*, volume 1B09, Aug. 2013.

[miyazaki-16:2013] H. Iwata, T. Miyazaki, and N. Suematsu. Schema in Cassandra for Large-scale Sensor Networks. In *IEEE student session in 2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers, Japan*, volume 1B09, Aug. 2013.

[miyazaki-17:2013] K. Kobayashi and T. Miyazaki. A Dynamic Role Assignment for Wireless Sensor Nodes. In *IEEE student session in 2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers, Japan*, volume 1B11, Aug. 2013.

[miyazaki-18:2013] N. Sagami and T. Miyazaki. A General Purpose 2D Array Processor. In *IEEE student session in 2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers, Japan*, volume 2B03, Aug. 2013.

[miyazaki-19:2013] S. Yamaguchi and T. Miyazaki. Development of Wireless Sensor Node using FPGA. In *IEEE student session in 2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers, Japan*, volume 2B04, Aug. 2013.

[miyazaki-20:2013] Y. Nishimaki and T. Miyazaki. A Customizable Visual Simulator for MIPS Processor. In *2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers*, volume 2G05, Aug. 2013.

[miyazaki-21:2013] N. Matsuura, T. Hata, T. Inoue, M. Takahashi, S. Takeuchi, D. Asahi, T. Kawasaki, H. Kurasawa, Y. Fujii, K. Harada, H. Sato, K. Takasugi, T. Nakamura, M. Kamiya,

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M. Nakamura, and T. Miyazaki. Practice and Evaluation of a Design Method for Field Trial of Real-world Services using Game at Event Place. In *2014 IEICE General Conference*, volume B-18-46, March 2014.

[miyazaki-22:2013] T. Hata, S. Takeuchi, H. Kawasaki, D. Asahi, M. Kamiya, K. Takasugi, H. Sato, and T. Miyazaki. Influence of Difference in Information Sharing on Groups in a Field Trial. In *2014 IEICE General Conference*, volume B-18-47, March 2014.

[miyazaki-23:2013] H. Kurasawa, Y. Fujii, H. Sato, A. Yamamoto, H. Kawasaki, M. Nakamura, M. Kamiya, A. Tsutsui, and T. Miyazaki. Evaluation of the Estimation for Missing Sensor Values Using a Field Trial. In *2014 IEICE General Conference*, volume B-18-48, March 2014.

[miyazaki-24:2013] T. Nakamura, N. Matsuura, K. Kashiwagi, D. Asahi, T. Inoue, Y. Fujii, H. Kurasawa, M. Nakamura, and T. Miyazaki. Storage Library for Sensor Log on Smartphone Applied to Field Trial Systems. In *2014 IEICE General Conference*, volume B-18-50, March 2013.

[miyazaki-25:2013] H. Iwata, N. Suematsu, and T. Miyazaki. Seamless Data-sharing for Constructing Large-scale Sensor Network. In *IPSSJ 76th National Convention*, volume 6W-2, March 2014.

[miyazaki-26:2013] Y. Watanabe, M. Ohta, and T. Miyazaki. Trajectory Pattern Analysis for Rambling Activities in Event Space. In *IPSSJ 76th National Convention*, volume 5V-8, March 2014.

[miyazaki-27:2013] Y. Nishimaki, J. Kitamichi, and T. Miyazaki. Implementation of Customizable Visual Simulator for MIPS Processor. In *IPSSJ 76th National Convention*, volume 3J-1, March 2014.

The student encouragement award

[miyazaki-28:2013] K. Ishikawa, N. Sagami, and T. Miyazaki. Arithmetic Precision of Time-space Continuous Dynamic Programming toward Its Dedicated Hardware. In *IPSSJ 76th National Convention*, volume 4K-4, March 2014.

Grants

- [hiroshis-07:2013] T. Hanyu H. Saito K. Kise T. Yoneda, M. Imai. Core Research for Evolutional Science and Technology of Japan Science and Technology Corporation, 2008-2013.
- [hiroshis-08:2013] H. Saito. Ministry of Education Scientific Research Fund, 2012-2014.
- [hiroshis-09:2013] H. Saito and Y. Kohira. Strategic Information and Communications R&D Promotion Programme (SCOPE), 2013-2014.
- [miyazaki-29:2013] T. Miyazaki. JSPS KAKENHI (Grants-in-Aid for Scientific Research), 2011-2013.
- [miyazaki-30:2013] T. Miyazaki. MIC Strategic Information and Communications R&D Promotion Programme (SCOPE), 2012-2014.
- [miyazaki-31:2013] T. Miyazaki. Joint research with NTT innovation laboratories, 2013.

Academic Activities

- [hiroshis-10:2013] H. Saito, September 2013.
Technical Program Committee member of IEEE MCSoc 2013.
- [miyazaki-32:2013] T. Miyazaki, 2012-2013.
IEEE Sendai Section, Executive Committee Member
- [miyazaki-33:2013] T. Miyazaki, 2013.
Steering Committee Member, IEICE Technical Group for Function Integrated Information System (FIIS)
- [miyazaki-34:2013] T. Miyazaki, 2013.
Steering Committee Member, MCSoc-13 (IEEE 8th International Symposium on Embedded Multicore Systems-on-Chip)
- [miyazaki-35:2013] T. Miyazaki, 2013.
Technical Program Committee Member, MobiPST (IEEE International Workshop on Privacy, Security and Trust in Mobile and Wireless Systems)
- [miyazaki-36:2013] T. Miyazaki, 2013.
Program Co-chair, SDSN2013 (International Workshop on Software Defined Sensor Networks)

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- [miyazaki-37:2013] T. Miyazaki, Feb. 2014.
Session Chair, ICNC2014 (IEEE International Conference on Computing, Networking, and Communications)
- [miyazaki-38:2013] T. Miyazaki, 1984 – present.
IEICE Member
- [miyazaki-39:2013] T. Miyazaki, 1986 – present.
IPSJ Member
- [miyazaki-40:2013] T. Miyazaki, 2012 – present.
IEEE Senior Member

Ph.D and Others Theses

- [hiroshis-11:2013] S. Iwasaki. Design and Evaluation of a Low Power Asynchronous AVR Processor considering a Cycle Time Constraint, University of Aizu, 2013.
Thesis Advisor: H. Saito
- [hiroshis-12:2013] S. Miyasono. Development of a Code Partitioning Tool for Network-on-Chip, University of Aizu, 2013.
Thesis Advisor: H. Saito
- [miyazaki-41:2013] Shunsuke Ito. Graduation Thesis: Graphical User Interface and a Mashup Server to Handle Huge Data Effectively in a Large-scale Sensor Network, University of Aizu, 2013.
Thesis Advisor: T. Miyazaki
- [miyazaki-42:2013] Daisuke Baba. Graduation Thesis: Emulation Environment for Nation-Wide Sensor Networks, University of Aizu, 2013.
Thesis Advisor: T. Miyazaki
- [miyazaki-43:2013] Naoki Suematsu. Graduation Thesis: Comparisons of Database Systems Targeting Huge Sensed Data Management, University of Aizu, 2013.
Thesis Advisor: T. Miyazaki
- [miyazaki-44:2013] Syun Nabeshima. Graduation Thesis: Role Activation Method for Programmable Wireless Sensor Node, University of Aizu, 2013.
Thesis Advisor: T. Miyazaki

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- [miyazaki-45:2013] Yuji Nishimaki. Master Thesis: Customizable Visual Simulator for MIPS Processor, University of Aizu, 2013.
Thesis Advisor: T. Miyazaki
- [miyazaki-46:2013] Koji Kobayashi. Master Thesis: Dynamically Reconfigurable Wireless Sensor Network, University of Aizu, 2013.
Thesis Advisor: T. Miyazaki
- [miyazaki-47:2013] Hiroki Iwata. Master Thesis: A Flexible Distributed Database System for Large-scale Sensor Networks, University of Aizu, 2013.
Thesis Advisor: T. Miyazaki
- [miyazaki-48:2013] Shoichi Yamaguchi. Master Thesis: Development of Reconfigurable Wireless Sensor Node Using Low-power FPGA, University of Aizu, 2013.
Thesis Advisor: T. Miyazaki