Computer Logical Design Laboratory

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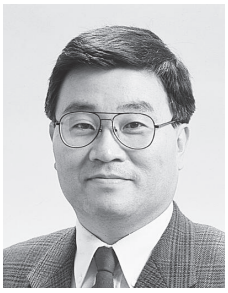

Robert H. Fujii
Senior Associate Professor

Yukihide Kohira
Associate Professor

Tsuneo Tsukahara:

Software-Defined Radio Transceivers

Related to this topic, the following work was done in 2013.

A High-Precision Quadrature Modulator and High-Performance RF Front-End Circuits suitable for Multi-band Wireless Transceivers:

Recently the demand for wireless systems such as sensor networks has been rapidly growing. However, radio-wave resources are limited and invaluable especially in these days. Therefore, software-defied radios (SDRs) and cognitive radios, which is a principal application of SDR, can be the key to greatly improving frequency-spectrum efficiency. SDRs demand flexibility and reconfigurability in RF (Radio Frequency) circuits. Therefore, a spectrum-efficient wireless transceiver architecture is indispensable. In this research, we proposed a multi-band wireless transceiver using a high-precision complex quadrature modulator (HP-CQMOD) and a flexible-filtering receiver suitable for sensor networks. As the final goal of our research, we would like to establish a reconfigurable wireless communicator, whose frequency band can be changed according to communication conditions and/or a country's regulations using reconfigurable RF and baseband processors and downloadable software. This is a kind of cognitive radios based on SDR (Software-Defined Radios). In recent years, multi-level modulations such as Quadrature Amplitude Modulation (QAM) are or will be used in Wireless LANs, digital TVs, and the 4th-generation cell-phones. So, very small modulation errors of QMOD are strongly demanded. In the 2013, we concen-

trated on circuit design of low-power HP-CQMODs and linear power amplifiers in the transmitter, and have started research on frequency-shift filtering methods. Moreover, we devised low-distortion receiver front-end circuits and designed digitally-controlled oscillators (DCOs) and time-to-digital converters (TDCs) for all-digital PLLs (ADPLL) for carrier-signal generation.

RF/IF building blocks we designed have three features as follows:

1. Low-power high-precision complex quadrature modulators are newly developed, featuring folded-cascode frequency divider used for a 90-dgree phase shifter and passive quadrature mixers.
2. We proposed linear CMOS power amplifiers using compensation techniques for transconductance and capacitance non-linearities.
3. Low-distortion and wideband techniques were devised for RF low-noise amplifiers and mixers.

Yukihide Kohira:

We investigate *design automation methodology for LSI circuits*. Due to the increase of scales of LSI circuits and the decrease of time to market of LSI products, design automation systems are widely used in order to design LSI circuits. Since the performance of LSI depends on the used design automation systems, it is important to develop design automation methodology continuously in order to obtain good products.

Our research interests are design automation for clock synchronous framework and layout design. In 2013, we focused on following four topics.

General-synchronous Framework

In general-synchronous framework, a clock is distributed periodically to all registers but the clock is not necessarily distributed simultaneously. General-synchronous framework is expected to obtain LSI circuits with high performance and low power consumption. The target of this research is to establish a design automation system for general-synchronous framework. In 2013, we investigated clock scheduling in which the number of clock domains is restricted to two to obtain circuits with high performance without increasing power consumption and an implementation method of circuits into FPGA in general-synchronous framework. In our experiments, circuits with higher performance were obtained by the proposed methods.

Deskew

In resent LSI circuits, process variations increase significantly because of the progress of the process technology. The process variations significantly cause delay variations and delay variations affect the performance and the yield of VLSI chips. If the circuit cannot work at the testing process after the fabrication of LSI chips, the circuit can be recovered by deskew in which delay of the programmable delay elements is adjusted. The target of this research is to establish a design automation system for deskew which can improve the yield of LSI chips. In 2013, we proposed the delay turning method in which the programmable delay elements with an ordered finite set of delay values and confirmed that the proposed method improved the yield.

Placement

In the recent LSI design, it is difficult to obtain a placement which satisfies both design constraints and specifications due to the increase of the circuit size, the progress of the manufacturing technology, and the speed-up of the circuit performance. Analytical placement methods are promising to obtain the placement which satisfies both design constraints and specifications. The target of this research is to establish a placement methodology to satisfy both design constraints and specifications in short computational time. In 2013, we proposed an acceleration method by GPGPU for an analytical placement method and confirmed that the proposed method was about ten times faster than the conventional sequential programming.

Lithography

Litho-Etch-Litho-Etch (LELE) type double patterning which seems to be most practical solution for the 22 nm node enables us to fabricate smaller features without using advanced technologies such as extreme ultraviolet (EUV) lithography. In LELE type double patterning, a layout pattern is decomposed and assigned to two masks so that each can be formed on a wafer by an exposure. The yield which affects manufacturing cost much depends on a layout pattern decomposition. A layout pattern decomposition method needs to have an ability to achieve higher yield. The target of this research is to establish a design automation system for advanced lithography such as LELE type double patterning to improve the yield. In 2013, we proposed a fast layout decomposition algorithm in LELE type double patterning considering the yield. Our proposed algorithm obtained a layout decomposition with mini-

mum cost efficiently for higher yield. In our experiments, our proposed algorithm was 7.7 times faster than an existing method on average.

Refereed Journal Papers

[kohira-01:2013] S. Kuwabara, Y. Kohira, and Y. Takashima. An Effective Overlap Removable Objective for Analytical Placement. *IEICE Trans. Fundamentals*, E96-A(6):1348–1356, 2013.

In the recent LSI design, it is difficult to obtain a placement which satisfies both design constraints and specifications due to the increase of the circuit size, the progress of the manufacturing technology, and the speed-up of the circuit performance. Analytical placement methods are promising to obtain the placement which satisfies both design constraints and specifications. Although existing analytical placement methods obtain the placement with the short wire length, the obtained placement has overlap. In this paper, we propose Overlap Removable Area as an overlap evaluation method for an analytical placement method. Experiments show that the proposed evaluation method is effective for removing overlap in the analytical placement method.

Refereed Proceeding Papers

[fujii-01:2013] “ M. Irifune and R.H. Fujii ”. “ Phase Control of Coupled Neuron Oscillators ”. In “ V. Mladenov, P. Koprinkova-Hristova, G. Palm, A. Villa, B. Apolloni, and N. K. Kasabov “ , editors, ” *International Conference on Artificial Neural Networks (ICANN) 2013*” ,, pages “ 296– 303 “ , “ Berlin Heidelberg ” , ” September ” 2013. “ European Neural Networks Society ” , “ Springer, Lecture Notes in Computer Science, Vol. 8131, Subseries: Theoretical Computer Science and General Issues ” .

“ The phase response of an Izhikevich neuron integrator/resonator model based oscillator to a weak short-duration input pulse is used to determine the Izhikevich model dynamic parameter values needed to attain a specified phase difference between coupled neuron oscillators working at the same natural oscillation frequency. The design of a new type of neuron oscillator-chain based artificial central pattern generator for the coordinated four-legged animal walking movement is proposed as an application. ”

[kohira-02:2013] Y. Yokoyama, K. Sakanushi, Y. Kohira, A. Takahashi, C. Kodama, S. Tanaka, and S. Nojima. Yield-aware decom-

position for LELE double patterning. In *SPIE Design-Process-Technology Co-optimization for Manufacturability VIII*, page DOI: 10.1117/12.2046263, February 2014.

Among several double patterning methods, Litho-Etch-Litho-Etch type DPT is known to have an advantage of layout flexibility. There are two problems when a hotspot, which is not fixable by tuning OPC, is detected on a wafer or during lithography compliance verification. One is to redo decomposition, OPC and verification is quite time consuming. The other is a risk to introduce a new hotspot at different locations. In this report, a new method to fix hotspot with layout modification of limited area will be presented. The proposed method can reduce not only repair turnaround time but also a risk of new hotspot generation.

[kohira-03:2013] S. Kuwabara, Y. Kohira, and Y. Takashima. An Acceleration Method by GPGPU for Analytical Placement using Quasi-Newton Method. In *IEEE 10th International Conference on ASIC (ASICON 2013)*, pages 472–475, October 2013.

In this paper, we propose an acceleration method by GPGPU for an analytical placement using a quasi-Newton method. In recent years, analytical placement methods are promising to obtain placements for circuits with many blocks. In the existing analytical placement methods using quasi-Newton methods, it takes huge execution time to evaluate the objective function and its gradient iteratively. In our proposed method, we accelerate the analytical placement method by parallelizing their calculation. Experiments show that our proposed method is effective by the comparison on the quality of the obtained placement and the execution time.

[kohira-04:2013] Y. Kohira, Y. Yokoyama, C. Kodama, A. Takahashi, S. Nojima, and S. Tanaka. Yield-aware decomposition for LELE double patterning. In *SPIE Design-Process-Technology Co-optimization for Manufacturability VIII*, page DOI: 10.1117/12.2046180, February 2014.

In this paper, we propose a fast layout decomposition algorithm in litho-etch-litho-etch (LELE) type double patterning considering the yield. Our proposed algorithm extracts stitch candidates properly from complex layouts including various patterns, line widths and pitches. The planarity of the conflict graph and independence of stitch-candidates are utilized to obtain a layout decomposition with minimum cost efficiently for higher yield. The validity of our proposed algorithm is confirmed by

using benchmark layout patterns used in literatures as well as layout patterns generated to fit the target manufacturing technologies as much as possible. In our experiments, our proposed algorithm is 7.7 times faster than an existing method on average.

[kohira-05:2013] H. Mashiko and Y. Kohira. A Tuning Method of Programmable Delay Element with Two Values for Yield Improvement. In *18th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2013)*, pages 159–164, October 2013.

Due to progressing the process technology in LSI and increasing variations of wire and gate delays after fabrication, timing violations cause significant reduction in the yield of LSI chips. To recover the timing violations, programmable delay elements called PDEs are inserted into the clock tree before fabrication and their delays are tuned after fabrication. In this paper, we use PDEs with two delay values and propose a delay tuning method of the PDEs to improve the yield and to reduce the number of tests. Moreover, we evaluate the circuits obtained by the proposed method by using commercial CAD tools. Experimental results show that the proposed method is effective.

[kohira-06:2013] Y. Kohira and A. Takahashi. 2-SAT Based Linear Time Optimum Two-Domain Clock Skew Scheduling. In *19th Asia and South Pacific Design Automation Conference (ASP-DAC 2014)*, pages 173–178, January 2014.

Multi-domain clock skew scheduling is an effective technique to improve the performance of sequential circuits by using practical clock distribution network. Although the upper bound of performance of a circuit increases as the number of clock domains increases in multi-domain clock skew scheduling, the improvement of the performance becomes smaller while the cost of clock distribution network increases much. In this paper, a linear time algorithm that finds an optimum two-domain clock skew schedule is proposed. Experimental results on ISCAS89 benchmark circuits and artificial data show that optimum circuits are efficiently obtained by our method in short time.

[tsuka-01:2013] S. Yamaguchi, T. Miyazaki, J. Kitamichi, S. Guo, T. Tsukahara, and T. Hayashi. Programmable Wireless Sensor Node Featuring Low-power FPGA and Microcontroller. In *The 6th IEEE International Conference on Ubi-Media Computing (UMEDIA2013)*, pages pp. 596–600, November 2013.

A sensor node often uses a low-performance microcontroller unit (MCU) to reduce its power consumption. However, it is difficult to handle heavy tasks with the MCU. To solve this problem, we developed a new sensor node that uses an ultra-low power field-programmable gate array (FPGA) in addition to an MCU.

[tsuka-02:2013] D. Zeng, Miyazaki T, Guo S, T. Tsukahara, J. Kitamichi, and T. Hayashi. Evolution of Software-Defined Sensor Networks. In *IEEE 9th International Conference on Mobile Ad-hoc and Sensor Networks (MSN 2013)*, pages pp. 410–413, December 2013.

After a decade of extensive research on application-specific wireless sensor networks (WSNs), the recent development of information and communication technologies make it practical to realize a new WSN paradigm, software-defined sensor network (SDSN), which is able to adapt to various application requirements and to fully explore the communication, computation and sensing resources of WSNs. We introduce the concept of SDSNs and outline several pioneering related work and enabling technologies for the realization of SDSNs.

[tsuka-03:2013] T. Miyazaki, S. Yamaguchi, K. Kobayashi, J. Kitamichi, S. Guo, T. Tsukahara, and T. Hayashi. A Software Defined Wireless Sensor Network. In *IEEE International Conference on Computing, Networking and Communications (ICNC2014)*, pages pp. 847–852, February 2014.

We propose a software-defined wireless sensor network system whose behavior can be redefined even after deployment by the injection of sensor node roles by means of wireless network communications. Two main technologies are used to develop this system, role generation and delivery mechanism, and a reconfigurable wireless sensor network with many reconfigurable sensor nodes.

[tsuka-04:2013] T. Miyazaki, H. Iwata, K. Kobayashi, S. Yamaguchi, S. Guo D. Zeng, J. Kitamichi, T. Hayashi, and T. Tsukahara. DASN: Demand-addressable Sensor Network for Active Information Acquisition. In *ACM the 8th International Conference on Ubiquitous Information Management and Communication (IMCOM2014)*, page DOI: 10.1145/2560000/2557995, January 2014.

In this paper, we propose a new type of sensor network called the demand-addressable sensor network (DASN). DASN actively gets desired information by delivering or addressing users ' demands to appropriate

places that are expected to have the information. This is in contrast to conventional sensor networks, which simply send sensed data to users. DASN is useful for finding desired information in a short amount of time from a large amount of sensed data generated by a large-scale sensor network.

Unrefereed Papers

[kohira-07:2013] Y. Kohira, Y. Takekawa, C. Kodama, A. Takahashi, S. Nojima, and S. Tanaka. Overlap Area Maximization in Stitch Selection for LELE Double Patterning. In *The 26th Workshop on Circuits and Systems*, pages 446–471, July 2013.

[kohira-08:2013] S. Kuwabara, Y. Kohira, and Y. Takashima. An Acceleration Improvement Method by GPGPU for Analytical Placement using Quasi-Newton Method. In *IEICE Society Conference (A-3-1)*, volume A, page 44, September 2013.

[kohira-09:2013] J. Kawaguchi and Y. Kohira. Technology Mapping for Low Power Consumption in General-Synchronous Framework. In *2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers (1C05)*, August 2013.

[kohira-10:2013] K. Yamazaki and Y. Kohira. A Longest Path Algorithm for Differential Pair Net Considering Connectivity. In *IEICE Technical Report (VLD2013-3)*, volume 113, pages 13–18, May 2013.

[kohira-11:2013] T. Masui and Y. Kohira. Implementation of General-Synchronous Circuits into FPGA using Multi-Domain Clock Skew Scheduling. In *IEICE Technical Report (VLD2013-167)*, volume 113, pages 183–188, March 2014.

[kohira-12:2013] K. Yamazaki and Y. Kohira. Local Pattern Modification Method for Lithographical ECO in Double Patterning. In *IEICE Technical Report (VLD2013-149)*, volume 113, pages 87–92, March 2014.

[kohira-13:2013] H. Mashiko and Y. Kohira. A Tuning Method of Programmable Delay Element with an Ordered Finite Set of Delay Values for Yield Improvement. In *IEICE Technical Report (VLD2013-99)*, volume 113, pages 275–280, November 2013.

[tsuka-05:2013] Y. Sato and T. Tsukahara. Distortion-Reduction Techniques for a 5-GHz-Band Two-Stage Power Amplifier. In *The 2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers*, August 2013.

[tsuka-06:2013] H. Takahashi and T. Tsukahara. A Low-Voltage Operation High-Precision Complex Quadrature Modulator. In *The 2013 Society Conference of IEE Japan (Electronics, Information, and Systems)*, September 2013.

Grants

[kohira-14:2013] Y. Kohira. Grant for Japanese Young Researchers from the Nakajima Foundation, 2013.

[kohira-15:2013] H. Saito and Y. Kohira. Strategic Information and Communications R&D Promotion Programme (SCOPE) from Ministry of Internal Affairs and Communications, 2013-2014.

[kohira-16:2013] A. Takahashi and Y. Kohira. Grants-in aid for Scientific Research (KAKENHI B) from Japan Society for the Promotion of Science (JSPS), 2013-2015.

[tsuka-07:2013] T. Tsukahara. Grants-in aid for Scientific Research (KAKENHI C) from JPSJ, 2011-2013.

[tsuka-08:2013] T. Tsukahara. Grant Donation from SANEI HYHTECS, 2013.

Academic Activities

[kohira-17:2013] Y. Kohira, October 2013.

Technical Program Committee Member, 18th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2013)

[kohira-18:2013] Y. Kohira, November 2013.

Organizing Committee Co-Chair, IEEE 5th International Conference on Awareness Science and Technology (iCAST2013) and IEEE 6th International Conference on Ubiquitous Multimedia (UMEDIA2013)

[kohira-19:2013] Y. Kohira, July 2013.

Program Committee Member, 26th Workshop on Circuits and Systems.

[kohira-20:2013] Y. Kohira, August 2013.

Financial Co-Chair, 2013 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers.

[tsuka-09:2013] T. Tsukahara, 2013.

Member of the IEICE Electronics Society Technical Committee on Integrated Circuits and Devices

[tsuka-10:2013] T. Tsukahara, 2013.

Secretary of the IEEJ Investigating R/D Committee on High-Frequency Integrated Circuits

Ph.D and Others Theses

[kohira-21:2013] Y. Maeda. Graduation Thesis: Iterative Improvement Method for Peak Power Reduction using 2-clustering in General-Synchronous Framework, University of Aizu, March 2014.

Thesis Advisor: Y. Kohira

[kohira-22:2013] S. Kuwabara. Master Thesis: Analytical Placement using Quasi-Newton Method and Acceleration by GPGPU, University of Aizu, March 2014.

Thesis Advisor: Y. Kohira

[kohira-23:2013] K. Saito. Graduation Thesis: Double Patterning Lithography Layout Decomposition Considering Balance, University of Aizu, March 2014.

Thesis Advisor: Y. Kohira

[kohira-24:2013] H. Mashiko. Master Thesis: A Tuning Method of Programmable Delay Element with an Ordered Finite Set of Delays for Yield Improvement, University of Aizu, March 2014.

Thesis Advisor: Y. Kohira

[kohira-25:2013] T. Oba. Graduation Thesis: Layout Design of General-Synchronous Circuits by Current CAD Tools, University of Aizu, March 2014.

Thesis Advisor: Y. Kohira

[kohira-26:2013] T. Masui. Master Thesis: Implementation of General-Synchronous Circuits into FPGA using Multi-Domain Clock Skew Scheduling, University of Aizu, March 2014.

Thesis Advisor: Y. Kohira

[tsuka-11:2013] Yuki Sato. Master thesis, Graduate School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara

[tsuka-12:2013] Hirota Takahashi. Master thesis, Graduate School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara

[tsuka-13:2013] Kimiaki Koinuma. Graduation thesis, School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara

[tsuka-14:2013] Chika Watanabe. Graduation thesis, School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara

[tsuka-15:2013] Ikko Tamura. Graduation thesis, School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara

[tsuka-16:2013] Natsumi Sato. Graduation thesis, School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara

[tsuka-17:2013] Ryo Ito. Graduation thesis, School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara

[tsuka-18:2013] Tomohiko Yokota. Graduation thesis, School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara

[tsuka-19:2013] Ryo Sugita. Graduation thesis, School of Computer Science and Engineering, February 2014.

Research adviser: T. Tsukahara