Adaptive Systems Laboratory

Ben Abdallah Abderazek
Senior Associate Professor

Yuichi Okuyama
Associate Professor

The academic area of this laboratory mainly covers computer design methodology. Reconfigurable computing, formal verification, network on a chip, and educational course design for VLSI are the major themes of this lab.

Short history of the Lab.:

"Computer Education Lab." started in 1993.

1993-1998 Prof. A. Taubin

2000-2012 Prof. K. Kuroda

2002- Prof. J. Kitamichi joined.

2005- Prof. Y. Okuyama joined.

2007- Prof. A. Ben joined.

2008- The title of the laboratory changed to "Adaptive Systems Lab.".

Members of our laboratory are three professors, 2 doctor program students, 8 master program students, and 4 (B4)+8(B3) graduate thesis students.

Education:

We have been developing an education program of VLSI design based on VDEC (VLSI Design and Education Center) support. VDEC offers various kinds of design tools without license costs and accepts chip fabrication orders in low price. This program was started as a joint research with Prof. Shima, who left from this university in 2004, in Computer Architecture Laboratory

in 2001. Web-based manuals for HDL design, verification, and layout tools have been developed and are being updated depending on VDEC support tools every year. Colaborating with Computer Organization Lab. and Logic Circuit Design Lab., we are establishing educational materials on embedded systems and FPGA-based design courseware.

Research: Recently, we are now focusing on the higher level design circumstances, such as UML, SystemC, and other HDLs. We developed a new design flow from SFL (one of the HDLs) to SystemC for improving the design efficiency. As to the VDEC-based synchronous circuit technology, various applications such as bio-informatics and network security have been surveyed.

We started a new approach to high performance computing systems with reconfigurable devices collaborating with the RIKEN research group, the PROGRAPE Project. The target of this project is “Desktop Supercomputing System”. “Desktop” means low-cost with commercially available FPGAs and PCs. We have been developing interface circuits and new applications such as fluid dynamics, data mining, and others. In collaboration with Prof. S. Sedukhin (Distr. Parallel Proc. Lab.), we have been developing a prototype of RapidMarix Processor System, which is a kind of torus array system specified for high performance matrix operation.

We also started a new approach to high performance computer architecture, "Queue Processor" and Network-on-Chip Architecure based on Prof. Ben's research background.

Members of the Adaptive Systems Laboratory

Prof. Junji Kitamichi:

He received the B.S. and Ph.D degrees in information and computer sciences from Osaka University, Japan, in 1988 and 1999, respectively. In 1991, he joined the Department of Information and Computer Sciences at Osaka University, Japan, as a research associate. ¿From 1999 to 2002, he was with Cybermedia Center at Osaka University, where he was assistant professor. In 2002, he joined School of Computer Science and Engineering, the University of Aizu, Japan. He was a professor at the University of Aizu from 2013. His research interests include formal methods for VLSI design, dynamically reconfigurable systems, formal design and verification of safety systems, heuristics and parallel algorithms for combinatorial optmization problems.

Prof. Abderazek Ben Abdallah:

He received his BTS degree from Sfax University in 1990. The BE, ME degrees from HUST Univ. in 1994 and 1997 respectively. In 2002, he received his Ph.D. degree from the Univ. of Electro-communications. From 2002 to 2007, he was a research associate at the Univ. of Electro-communications, Graduate School of Information Systems, then Assistant Professor at the network computing laboratory. He joined the Univ. of Aizu in 2007. His research interests span the areas of computer systems, embedded systems, and VLSI.

Prof. Yuichi Okuyama:

He was born in 1975. He received the M.S and Ph.D degrees in computer science and engneering from the University of Aizu in 1999 and 2002, respectively. He entered NTT Network Innovation Laboratories and was engaged with the development of PCA (Plastic Cell Architecture) devices. He joined the University of Aizu in 2005 as an assistant professor. His current interests are implementation of applications on hardware, tool development for design automation on reconfigurable device(FPGA and other devices) and design of hardware for scientific calculations.

Students :

Doctor Program:

D2: Akram Ben Ahmed.. D1: Achraf Ben Ahmed..

Master Program:

M2:Ryosuke Kaji, Yoshiaki Kondo, Toshihiro sato, Yoshuke Haraguchi.

M1:Kazuji Kobayashi, Toshiichi Idonuma, Takaaki Ouchi, Toru Hasegawa.

Graduation Thesis Students:

B4:Mitsuhiro Nakamura, Shoji Hashimoto, Shunshuke Baba, Shomu Ito.

B3:Taiga Hayase, Mitsunari Ishii, Hiroki Tanaka, Maiko Tanaka, Yusuke Sato, Syun Hayamizu, Kosuke Hongo, Shunsuke Ishikuro

Refereed Journal Papers

[benab-01:2013] A. Ben Abdallah Akram Ben Ahmed. Architecture and Design of High-throughput, Low-latency and Fault Tolerant Routing Algorithm for 3D-Network-on-Chip. *The Jnl. of Supercomputing*, 66(3):1507–1532, 12 2013.
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Refereed Proceeding Papers

[benab-02:2013] A. Ben Abdallah Achraf Ben Ahmed. PHENIC: Towards Photonic 3D-Network-on-Chip Architecture for High-throughput Many-core Systems-on-Chip. In *IEEE Proceedings of the 14th International conference on Sciences and Techniques of Automatic control and computer engineering*, pages 1–6. IEEE, 12 2013.
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[benab-03:2013] A. Ben Abdallah Akram Ben Ahmed, Achraf Ben Ahmed. Deadlock-Recovery Support for Fault-tolerant Routing Algorithms in 3D-NoC Architectures. In *IEEE Proceedings of the 7th International Symposium on Embedded Multicore/Many-core SoCs (MCSoC-13),*, pages 67–72. IEEE, 9 2013.
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[benab-04:2013] A. Ben Abdallah Achraf Ben Ahmed. Hardware/Software Prototyping of Dependable Real-Time System for Elderly Health Monitoring. In *Proc. of the World Congress on Computer and IT (ICMAES)*, pages 1–6. ICMAES, 6 2013.
.

[benab-05:2013] S. Miura A. Ben Abdallah Akram Ben Ahmed, T. Ouchi. Run-Time Monitoring Mechanism for Efficient Design of Application-specific NoC Architectures in Multi/Manycore Era. In 7, editor, *IEEE Proc. of the 6th International Workshop on Engineering Parallel and Multicore Systems (ePaMuS2013)*, pages 440–445, 2013.
.

[okuyama-01:2013] Toshihiro Sato, Yuichi Okuyama, and Motoki Sakai. Simulation Study of a P300 Speller for Single-Lead Hybrid BCI.

In Editor M.P. Bekakos, editor, *SICE Annual Conference 2013 (SICE2013)*, page TuAT12.1, Nagoya, Japan, April, 2013. SICE, Cambridge Univercity Press.

Young Author's Award Finalist

Unrefereed Papers

[okuyama-02:2013] 加治良亮 and 奥山祐市. データ転送量削減を主眼としたGPGPU による 2DCDP 実装の高速化. In *2013* 年度情報処理学会東北支部研究会, pages 13–7–A3–2, Yamagata, Japan, March 2014.

[okuyama-03:2013] Yosuke Haraguchi and Yuichi Okuyama. A Parallelization Approach for Affine-Scale-invariant Feature Transform Using MPI. In *2013* 年度情報処理学会東北支部研究会, pages 13–7–A3–3, Yamagata, Japan, March 2014.

[okuyama-04:2013] Toshihiro Sato and Yuichi Okuyama. Evaluation of Arithmetic Precision for Single-lead Hybrid BCI Hardware Using P300 Speller. In *2013* 年度情報処理学会東北支部研究会, pages 13–7–A3–4, Yamagata, Japn, March 2014.

[okuyama-05:2013] 奥山祐市 橋本将司. ストリーミング言語を用いた 2DCDP プロセッサのノード間コミュニケーションの考察. In *2013* 年度情報処理学会東北支部研究会, pages 13–7–A4–1, March 2014.

[okuyama-06:2013] 馬場俊助 and 奥山祐市. 多電極 ECG 解析のためのスレッドベースのリアルタイム処理の実験. In *2013* 年度情報処理学会東北支部研究会, pages 13–7–A4–2, Yamagata, Japan, March 2014.

[okuyama-07:2013] 中村光宏 and 奥山祐市. 行列 FMA 内のネットワークの性能評価. In *2013* 年度情報処理学会東北支部研究会, pages 13–7–A4–3, Yamagata, Japan, March 2014.

[okuyama-08:2013] 伊藤翔夢, 奥山祐市, and 酒井元気. AdaBoosted SVM を用いた脳波からの計算能力の習得に関する実験. In *2013* 年度情報処理学会東北支部研究会, pages 13–7–A4–4, Yamagata, Japan, March 2014.

[okuyama-09:2013] 小林 一樹, 白井 凱将, 中村 光宏, and 奥山 祐市. FPGA を用いた行列演算器のための入出力回路の実装. In 平成 *25* 年度 第 *5* 回情報処理学会東北支部研究会開催報告, page [20], Fukushima, Japan, Jan. 2014.

[okuyama-10:2013] 井戸沼 俊市, 矢口 勇一, and 奥山 祐市. 2DCDP における累積値ハードウェアの実装. In 平成 *25* 年度 第 *5* 回情報処理学会東北支部研究会開催報告, page [21], Fukushima, Japan, Jan. 2014.

[okuyama-11:2013] 大内 高章 and 奥山 祐市. FPGA における 2DCDP プロセッサのための分散 RAM の評価. In 平成 *25* 年度 第 *5* 回情報処理学会東北支部研究会開催報告, page [22], Fukushima, Japan, Jan. 2014.

[okuyama-12:2013] 長谷川 徹, 伊藤 翔夢, 酒井 元気, and 奥山 祐市. SVM を用いた脳波による加算処理能力推定のためのデータ分析手法の提案. In 平成 *25* 年度 第 *5* 回情報処理学会東北支部研究会開催報告, page [22], Fukushima, Japan, Jan. 2014.

[okuyama-13:2013] 長谷川徹, 奥山祐市, and 酒井元気. 汎用的な EEG-Based Biofeedback の実装手法の提案. In 平成 *25* 年度電気関係学会東北支部連合大会, page 2F22, Fukushima, Japan, Aug. 2013.

[okuyama-14:2013] 大内高章 and 奥山祐市. 2DCDP バックトレース回路の提案. In 平成 *25* 年度電気関係学会東北支部連合大会, page 2F21, Fukushiama, Japan, Aug. 2013.

[okuyama-15:2013] 井戸沼俊市 and 奥山祐市. 2DCDP 累積値計算部分のハードウェア実装とその評価. In 平成 *25* 年度電気関係学会東北支部連合大会, page 2F22, Fukushima, Japan, Aug. 2013.

Books

[benab-06:2013] A. Ben Abdallah. *Multicore Systems-on-Chip: Practical Hardware/Software Design, 2nd Edition*. Number ISBN-13: 978-9491216916. in Atlantis Ambient and Pervasive Intelligence. Atlantis, 2nd edition, 2013.
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Grants

[benab-07:2013] A. Ben Abdallah. High-Radix Network-on-Chip Architecture for Future Many-Core Systems, Competitive Research Funding,, 2013.

Academic Activities

[benab-08:2013] A. Ben Abdallah, 2013.

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[benab-09:2013] A. Ben Abdallah, 2013.

(1)Track Chair of Parallel Computing and Multicore Systems, 16th International Conference on Network-Based Information Systems (NBiS 2013), September 4-6, 2013, Gwangju, Korea. (2) Steering Chair, IEEE 7th International Symposium on Embedded Multicore/Manycore SoCs, (MCSoC 2013), National Center of Sciences, Tokyo, Japan, September 26-28, 2013. (3)Treasure and Secretary, ACM Chapter on E-learning and Technical Communication, 2013-2014. (4) TPC member of 6th International Workshop on Engineering Parallel and Multicore Systems, July 3-5, 2013, Taichung, Taiwan (5) TPC member of IEEE Symposium on Low-power and High-speed Chips (COOL Chips XI), Yokohama, April 17-19, 2013. (6) Guest Editor, Special Issue on Embedded Multicore and Many-core Architectures, Journal of Embedded Systems (IJES), 2013. (7) Editor, Journal of Adaptive and Innovative Systems, InderScience, 2013- (8) Editor, Journal of Embedded Systems, InderScience, 2013- (9) TPC member of Computers, Communications and IT Applications Conference (ComComAp 2013, HKUST, Hong Kong, April 1-4, 2013.

[okuyama-16:2013] Yuichi Okuyama, April 2013.

executive member

[okuyama-17:2013] Yuichi Okuyama, April 2013.

Regular mamber

[okuyama-18:2013] Yuichi Okuyama, April 2013.

CPSY steering committee

[okuyama-19:2013] Yuichi Okuyama, April 2013.

regular member

Patents

[benab-10:2013] A. Ben Abdallah. A 3D-IC having the same, and a method for controlling the fault tolerant router, 2013.

Ph.D and Others Theses

[okuyama-20:2013] Mitsuhiro Nakamura. Graduation Thesis: Performance Evaluation of networks in Matrix FMA, University of Aizu, 2014.

Thesis Advisor: Y. Okuyama

[okuyama-21:2013] Masashi Hashimoto. Graduation Thesis: Implementation of Inter-node Communication in 2DCDP Processor Using Stream Language, University of Aizu, 2014.

Thesis Advisor: Y. Okuyama

[okuyama-22:2013] Shunsuke Baba. Graduation Thesis: A Thread-based Real Time Processing for Multi-lead ECG Analysis, University of Aizu, 2014.

Thesis Advisor: Y. Okuyama

[okuyama-23:2013] Sean Ito. Graduation Thesis: Estimation of Calculation Capability from EEG Using AdaBoosted SVMs, University of Aizu, 2014.

Thesis Advisor: Y. Okuyama

[okuyama-24:2013] Toshihiro Sato. Master Thesis: Accuracy Analysis of Nonlinear State Space Projection Using P300 Speller for Single-lead Hybrid BCI Hardware, University of Aizu, 2014.

Thesis Advisor: Y. Okuyama

[okuyama-25:2013] Yosuke Haraguchi. Master Thesis: A Parallelization Approach for Affine Scale-invariant Feature Transform Using MPI, University of Aizu, 2014.

Thesis Advisor: Y. Okuyama

[okuyama-26:2013] Ryosuke Kaji. Master Thesis: Implementation of 2DCDP Backtracking on GPGPU, University of Aizu, 2014.

Thesis Advisor: Y. Okuyama

Others

[benab-11:2013] A. Ben Abdallah.

I organized the annual IEEE 7th International Symposium on Embedded Multicore/Manycore SoCs, (MCSoC 2013), National Center of Sciences, Tokyo, Japan, September 26-28, 2013.