Embedded Systems Laboratory

Junji Kitamichi
Professor

The Embedded Systems Laboratory was established in July, 2013. Embedded systems are products which computers are embedded, and the research region of the embedded systems is very wide, such as software, hardware, and middle-ware, from theory to application, calculation performance, power consumption, safety, and development methods. We are researching the following themes out of many research topics about embedded systems.

1. Safety Embedded System

(a) Formal Approach for Circuits Design and Systems Design

(b) Design Method at System Design Level

2.Dynamically Reconfigurable Architectures and Systems

3.Heuristic Approaches for Combinatorial Optimization Problems

4.Education of Circuits Design, Embedded Systems and Computer Architecture

Members of the Embedded Systems Laboratory

Prof. Junji Kitamichi:

He received the B.S. and Ph.D degrees in information and computer sciences from Osaka University, Japan, in 1988 and 1999, respectively. In 1991, he joined the Department of Information and Computer Sciences at Osaka University, Japan, as a research associate. From 1999 to 2002, he was with Cybermedia Center at Osaka University, where he was assistant professor.

In 2002, he joined School of Computer Science and Engineering, the University of Aizu, Japan. He was a professor at the University of Aizu from 2013. His research interests include formal methods for VLSI design, dynamically reconfigurable systems, formal design and verification of safety systems, heuristics and parallel algorithms for combinatorial optimization problems.

Students :

B3:Souichirou Endou, Kazumi Hoshi.

Refereed Journal Papers

[kitamiti-01:2013] Junji KITAMICHI Yuji NISHIMAKI and Toshiaki MIYAZAKI. Development of Education-purpose MIPS Processor Simulator System Visualizing Internal Operation Behavior. *IEICE TRANSACTIONS on Information and Systems*, J96-D(10):2130–2138, 2013.

This paper proposes a processor simulator expected to be used in lectures and/or exercises, which are aimed at teaching computer architecture. The target of the simulator is beginners who have basic knowledge and skill to develop simple software programs, but not have deep hardware knowledge. Historically, many processor simulators have been proposed, but they only support the instruction-level simulation. Thus, it is hard for the beginners to understand hardware parallelism and how each instruction is executed in a processor, even if they use the simulators. The proposed processor simulator can simulate several variations of MIPS processor architecture, and visualize their internal behaviors using some windows showing different aspects of the instruction execution. The evaluation results using some students show that the proposed simulator is useful for the beginners, compared to other methods for teaching computer architecture.

Refereed Proceeding Papers

[kitamiti-02:2013] Junji Kitamichi Shuta Yamamoto. A Combinatorial Algorithm of Ant Colony Optimization and Neural Network Algorithm for Channel Assignment Problem. In *2013 International Symposium on Nonlinear Theory and its Applications (NOLTA2013)*, pages A3L–C. Nonlinear Theory and Its Applications, IEICE, IEICE, Sep. 2013.

Recently, demands for cellular radio network are increasing cellular devices such as smart phones or wireless sensor devices. Channel Assignment Problem(CAP) are becoming more important in order to make the most of limited channels. This paper proposes a combined method of Ant Colony Optimization and Neural Network Algorithm for the CAP. The proposed method can achieve similar solution ability in some instances, and can acquire 2% smaller interference solution in 3 benchmarks in average and the

same interference solutions in 2 benchmarks compared with an existing method.

Unrefereed Papers

[kitamiti-03:2013] Junji KITAMICHI Yuji NISHIMAKI and Toshiaki MIYAZAKI. Implementation of Customizable Visual Simulator for MIPS Processor. In IPSJ, editor, *The 76th National Convention of IPSJ*, pages 3J–1. IPSJ, IPSJ, March 2014.

Academic Activities

[kitamiti-04:2013] Kitamichi J., 2013.
Member. IEEE

[kitamiti-05:2013] Kitamichi J., 2013.
Member, IPSJ

[kitamiti-06:2013] Kitamichi J., 2013.
Member, IEICE. Steering Comittee Member, Tohoku Branch, IEICE