Computer Logical Design Laboratory

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Tsuneo Tsukahara:

Software-Defined Radio Transceivers

Related to this topic, the following work was done in 2014.

A High-Precision Quadrature Modulator and High-Performance RF Front-End Circuits suitable for Multi-band Wireless Transceivers:

Recently the demand for wireless systems such as sensor networks has been rapidly growing. However, radio-wave resources are limited and invaluable especially in these days. Therefore, software-defied radios (SDRs) and cognitive radios, which is a principal application of SDR, can be the key to greatly improving frequency-spectrum efficiency. SDRs demand flexibility and reconfigurability in RF (Radio Frequency) circuits. Therefore, a spectrum-efficient wireless transceiver architecture is indispensable. In this research, we proposed a multi-band wireless transceiver using a high-precision complex quadrature modulator (HP-CQMOD) and a flexible-filtering receiver suitable for sensor networks. As the final goal of our research, we would like to establish a reconfigurable wireless communicator, whose frequency band can be changed according to communication conditions and/or a country ' s regulations using reconfigurable RF and baseband processors and downloadable software. This is a kind of cognitive radios based on SDR (Software-Defined Radios). In recent years, multi-level modulations such as Quadrature Amplitude Modulation (QAM) are or will be used in Wireless LANs, digital TVs, and the 4th-generation cell-phones. So, very small modulation errors of QMOD are strongly demanded. In the 2014, we concentrated on circuit design of low-power HP-CQMODs and linear power amplifiers in the trans-

mitter, and have started research on RF-band complex bandpass filtering and frequency-shift filtering methods. Moreover, we devised low-distortion receiver front-end circuits and designed digitally-controlled oscillators (DCOs) suitable for all-digital PLLs (ADPLL) and sub-sampling PLL architectures for generating low-phase-noise carrier-signals.

RF/IF building blocks we designed have three features as follows:

1. Low-power high-precision complex quadrature modulators are newly developed, featuring a dual-LO switching quadrature mixer and an RF-band complex bandpass filter.
2. We proposed high-efficiency CMOS power amplifiers using a class-D mode.
3. Low-distortion and wideband techniques were devised for RF low-noise amplifiers and mixers.
4. Low-power class-D inductor-based oscillators suitable for DCOs.

Yukihide Kohira:

We investigate *design automation methodology for LSI circuits*. Due to the increase of scales of LSI circuits and the decrease of time to market of LSI products, design automation systems are widely used in order to design LSI circuits. Since the performance of LSI depends on the used design automation systems, it is important to develop design automation methodology continuously in order to obtain good products.

Our research interests are design automation for clock synchronous framework and layout design. In 2014, we focused on following four topics.

General-synchronous Framework

In general-synchronous framework, a clock is distributed periodically to all registers but the clock is not necessarily distributed simultaneously. General-synchronous framework is expected to obtain LSI circuits with high performance and low power consumption. The target of this research is to establish a design automation system for general-synchronous framework. In 2014, we investigated clock scheduling in which the number of clock domains is restricted to two to obtain circuits with high performance without increasing power consumption and an implementation method of circuits into FPGA in general-synchronous framework. Moreover, we investigated technology mapping in which assigns a cell in cell libraries to each gate. Our proposed

method realized both the performance improvement and the power consumption reduction. In our experiments, circuits with higher performance and lower power consumption were obtained by the proposed methods.

Deskew

In resent LSI circuits, process variations increase significantly because of the progress of the process technology. The process variations significantly cause delay variations and delay variations affect the performance and the yield of VLSI chips. If the circuit cannot work at the testing process after the fabrication of LSI chips, the circuit can be recovered by deskew in which delay of the programmable delay elements is adjusted. The target of this research is to establish a design automation system for deskew which can improve the yield of LSI chips. In 2014, we proposed the delay turning method in which the programmable delay elements with an ordered finite set of delay values and confirmed that the proposed method improved the yield.

PCB routing

Due to the increase of operation frequency, signal propagation delay is requested to achieve a specification with very high accuracy. Since the quality of the routing pattern obtained by automatic routing tools is inferior to the routing pattern obtained by designers, the routing pattern for high density routing is still obtained by hands. However, since the number of nets on a PCB and package has increased and the specification becomes severe, the manual design approaches the limit. The goal of this research is to establish automatic routing tools. In 2014, we proposed an acceleration method for an any-angle gridless routing method by GPGPU.

Lithography

Multiple patterning technique enables us to fabricate small features without using advanced technologies such as extreme ultra violet (EUV) lithography. Triple patterning lithography is one of the most promising techniques in 14 nm logic node and beyond. Two types of triple patterning technologies are often discussed in literature. In LELELE, litho-etch process is repeated three times. In LELECUT, the third mask called cut process removes a part of a fabricated pattern. It is used to improve the quality of fabricated patterns as well as to enhance the flexibility of layout. In 2014, we proposed a fast layout decomposition algorithm in LELELE and LELECUT by using positive semidenite relaxation.

Refereed Journal Papers

[kohira-01:2014] Y. Kohira and A. Takahashi. 2-SAT based Linear Time Optimum Two-Domain Clock Skew Scheduling in General-Synchronous Framework. *IEICE Trans. Fundamentals*, E97-A(12):2459–2466, 2014.

Multi-domain clock skew scheduling in general-synchronous framework is an effective technique to improve the performance of sequential circuits by using practical clock distribution network. Although the upper bound of performance of a circuit increases as the number of clock domains increases in multi-domain clock skew scheduling, the improvement of the performance becomes smaller while the cost of clock distribution network increases much. In this paper, a linear time algorithm that finds an optimum two-domain clock skew schedule in general-synchronous framework is proposed. Experimental results on ISCAS89 benchmark circuits and artificial data show that optimum circuits are efficiently obtained by our method in short time.

[kohira-02:2014] H. Mashiko and Y. Kohira. A Tuning Method of Programmable Delay Element with an Ordered Finite Set of Delays for Yield Improvement. *IEICE Trans. Fundamentals*, E97-A(12):2443–2450, 2014.

Due to the progress of the process technology in LSI, the yield of LSI chips is reduced by timing violations caused by delay variations. To recover the timing violations, delay tuning methods insert programmable delay elements called PDEs into the clock tree before fabrication and tune their delays after fabrication. The yield improvement of existing methods is not enough. In this paper, a delay tuning method of PDEs with an ordered finite set of delays is proposed for the yield improvement. The proposed delay tuning method is based on the modified Bellman-Ford algorithm. Therefore, its optimality is guaranteed and its time complexity is polynomial. In the experiments under Monte-Carlo simulation, the yield of the proposed method is improved higher when the number of delays in each PDE is increased.

Refereed Proceeding Papers

[kohira-03:2014] T. Honda and Y. Kohira. An Acceleration for Any-Angle Routing using Quasi-Newton Method on GPGPU. In *IEEE 8th International Symposium on Embedded Multicore/Manycore SoCs (MCSoC 2014)*, pages 281–288, September 2014.

In PCB routing and package routing, routes must satisfy various constraints and specifications. In recent years, an any-angle routing using a quasi-Newton method has been proposed to obtain a routing pattern satisfying the constraints and specifications. However, computational time of the quasi-Newton method is long because many computations are iterated for the evaluation of the objective function and its gradient. In this paper, we propose an acceleration method for the any-angle routing using a quasi-Newton method by GPGPU. Moreover, we also propose an improved method by omitting the redundant calculation of the evaluation of the objective function. Experiments show that the proposed method is effective by the comparison on the quality of obtained routes and the computational time

[kohira-04:2014] T. Matsui, Y. Kohira, C. Kodama, and A. Takahashi. Positive Semidefinite Relaxation and Approximation Algorithm for Triple Patterning Lithography. In *The 25th International Symposium on Algorithms and Computation (ISAAC 2014), (Algorithms and computation, Lecture Notes in Computer Science, LNCS 8889)*, pages 365–375, December 2014.

Triple patterning lithography (TPL) is one of the major techniques for 14 nm technology node and beyond. This paper discusses TPL layout decomposition which maximizes objective value representing decomposition quality. We introduce a maximization problem of the weighted sum of resolved conflicts and unused stitch candidates. We propose a polynomial time (7/9)-approximation algorithm based on positive semidefinite relaxation and randomized rounding procedure. Our algorithm returns a decomposition such that the expectation of the corresponding objective value is at least (7/9) times the optimal value even in the worst case problem instance. To our knowledge, the result is the first approximation algorithm with a constant approximation ratio for TPL.

[kohira-05:2014] Y. Kohira, T. Matsui, Y. Yokoyama, C. Kodama, A. Takahashi, S. Nojima, and S. Tanaka. Fast Mask Assignment using Positive Semidefinite Relaxation in LELECUT Triple Patterning Lithography. In *The 20th Asia and South Pacific Design Automation Conference (ASP-DAC 2015)*, pages 665–670, Januaryr 2015.

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[kohira-06:2014] J. Kawaguchi and Y. Kohira. Technology Mapping Method for Low Power Consumption and High Performance in General-Synchronous Framework. In *The 19th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2015)*, pages 665–670, March 2015.

In general-synchronous framework, in which the clock is distributed periodically to each register but not necessarily simultaneously, circuit performance is expected to be improved compared to complete-synchronous framework, in which the clock is distributed periodically and simultaneously to each register. To improve the circuit performance more, logic circuit synthesis for general-synchronous framework is required. In this paper, under the assumption that any clock schedule is realized by an ideal clock distribution circuit, when two or more cell libraries are available, a technology mapping method which assigns a cell to each gate in the given logic circuit by using integer linear programming is proposed. In experiments, we show the effectiveness of the proposed technology mapping method.

[kohira-07:2014] Y. Kohira, C. Kodama, T. Matsui, A. Takahashi, S. Nojima, and S. Tanaka. Yield-aware mask assignment using positive semidefinite relaxation in LELECUT triple patterning. In *SPIE Design-Process-Technology Co-optimization for Manufacturability VIII*, page DOI: 10.1117/12.2085285, February 2015.

LELECUT type triple patterning lithography is one of the most promising techniques in the next generationlithography. To prevent yield loss caused by overlay error, LELECUT mask assignment which is tolerant to overlay error is desired. In this paper, we propose a method that obtains an LELECUT assignment which is tolerant to overlay error. The proposed method uses positive semidefinite relaxation and randomized rounding technique. In our method, the cost function that takes the length of boundary of features determined by the cut mask into account is introduced.

Unrefereed Papers

[kohira-08:2014] H. Mashiko and Y. Kohira. Area Minimization of One-Dimensional Layout for MOS Circuits by SAT Solver and Simulated Annealing. In *IEICE Technical Report (VLD2014-158)*, volume 114, pages 31–36, March 2015.

[kohira-09:2014] Y. Moriai, M. Nakajima, S. Hosaka, Y. Kohira, and H. Saito. Visualization of Snow Depth by a Sensor Network. In *IEICE General Conference (B-18-40)*, volume B, page 587, March 2015.

[kohira-10:2014] J. Kawaguchi and Y. Kohira. Technology Mapping Method for Low Power Consumption and High Performance in General-Synchronous Framework. In *IEICE Technical Report (VLD2014-83)*, volume 114, pages 87–92, November 2014.

[kohira-11:2014] Y. Kohira, T. Matsui, Y. Yokoyama, C. Kodama, A. Takahashi, S. Nojima, and S. Tanaka. LELECUT Triple Patterning Lithography Layout Decomposition using Positive Semidefinite Relaxation. In *IEICE Technical Report (VLD2014-6)*, volume 114, pages 27–32, May 2014.

[kohira-12:2014] Takahashi A, A. Awad, Y. Kohira, T. Matsui, C. Kodama, S. Nojima, and S. Tanaka. [Invited] Multi Patterning Techniques for Manufacturability Enhancement in Optical Lithography. In *The 2014 International Conference on Integrated Circuits, Design, and Verification (ICDV 2014)*, pages 117–122, November 2014.

[kohira-13:2014] S. Hosaka, Y. Moriai, M. Nakajima, Y. Kohira, and H. Saito. Development of a Sensor Network to Measure Snow Depth using Arduino. In *IEICE Technical Report (ASN2014-45)*, volume 114, pages 31–36, July 2014.

[tsuka-01:2014] M. Ugajin, Y. Kobayashi, and T. Tsukahara. Study of High-Image-Rejection Wireless-Receiver Architecture Using 3-Pahse RC Complex Band Pass Filter. In *The 37th Technical Meetings on Analog RF*, December 2014.

[tsuka-02:2014] R. Ito and T. Tsukahara. A High-Precision Complex Quadrature Modulator Using a High-Frequency Complex Bandpass Filter. In *The Technical Meetings on Electronic Circuits, IEE Japan*, January 2015.

[tsuka-03:2014] T. Nishiuchi and T. Tsukahara. Design of RF CMOS Wideband Receiver Front-End. In *The 3rd JPSJ Tohoku-Branch Technical Meeting*, January 2015.

[tsuka-04:2014] M. Hotta, T. Tsukahara, and Y. Yuminaka. Activity Report of Investigating R/D Committee on Forefront Technology and Applications of High-Frequency Integrated Circuits. In *The Technical Meetings on Electronic Circuits, IEE Japan*, March 2015.

[tsuka-05:2014] T. Tsukahara. Fundamentals of Frequency Conversion and Modulation/Demodulation Indispensable for Wireless Communication Systems [Invited]. In *2014 Microwave Workshops and Exhibition (MWE2014)*, December 2014.

Chapters in Book

[tsuka-06:2014] T. Tsukahara. *Translation of Chapter 11 of RF Microelectronics (2nd Edition) by B. Razavi*, pages pp. 347–389. Maruzen, 2015.

Grants

[kohira-14:2014] H. Saito and Y. Kohira. Strategic Information and Communications R&D Promotion Programme (SCOPE) from Ministry of Internal Affairs and Communications, 2013-2014.

[kohira-15:2014] A. Takahashi and Y. Kohira. Grants-in aid for Scientific Research (B) from Japan Society for the Promotion of Science (JSPS), 2013-2015.

[kohira-16:2014] Y. Kohira. Grant-in-Aid for Young Scientists (B) from Japan Society for the Promotion of Science (JSPS), 2014-2016.

[tsuka-07:2014] M. Ugajin and T. Tsukahara. Grants-in aid for Scientific Research (KAKENHI C) from JSPS, 2014.

Academic Activities

[kohira-17:2014] Y. Kohira, August 2014.

Program Committee Member, 27th Workshop on Circuits and Systems

[kohira-18:2014] Y. Kohira, 2014.

Committee Member, IEICE Technical Committee on VLSI Design Technologies (VLD)

[kohira-19:2014] Y. Kohira, July 2014.

Associate Editor, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Special Section on Design Methodologies for System on a Chip

[kohira-20:2014] Y. Kohira, September 2014.

Publication Chair, IEEE 8th International Symposium on Embedded Multicore SoCs (MCSoC)

[kohira-21:2014] Y. Kohira, January 2015.

Liaison with ASPDAC 2015 Organizing Committee and Confirmed Committee Member, ACM SIGDA Student Research Forum at ASPDAC 2015

[kohira-22:2014] Y. Kohira, March 2015.

Technical Program Committee Member, 19th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2015)

[tsuka-08:2014] T. Tsukahara, 2014.

Member of the IEICE Electronics Society Technical Committee on Integrated Circuits and Devices

[tsuka-09:2014] T. Tsuakahara, 2014-2016.

Chair of the IEEJ Investigating R/D Committee on New Application Fields and Supporting Technology of High-Frequency Integrated Circuits

Patents

[tsuka-10:2014] T. Tsukahara. Complex Quadrature Modulator and Demodulator, and Applicable Quadrature Mixers, Japanese Patent 5574293, 2014.

Ph.D and Others Theses

[kohira-23:2014] J. Kawaguchi. Master Thesis: Technology Mapping Method for Low Power Consumption in General-Synchronous Framework, University of Aizu, March 2015.

Thesis Advisor: Y. Kohira

[kohira-24:2014] M. Terada. Graduation Thesis: Iterative Improvement Method for Peak Power Reduction using Multi-Clustering Method in General-Synchronous Framework, University of Aizu, March 2015.

Thesis Advisor: Y. Kohira

[kohira-25:2014] K. Uchida. Graduation Thesis: Improvement of Design Flow for FPGA Implementation in General-synchronous Framework, University of Aizu, March 2015.

Thesis Advisor: Y. Kohira

[kohira-26:2014] K. Hamatani. Graduation Thesis: Enhancement of Routing Method using Quasi-Newton Method, University of Aizu, March 2015.

Thesis Advisor: Y. Kohira

[kohira-27:2014] T. Honda. Master Thesis: Acceleration for Any-Angle Routing using Quasi-Newton Method on GPGPU, University of Aizu, March 2015.

Thesis Advisor: Y. Kohira

[tsuka-11:2014] Ryuji Kuroda. Graduation Thesis: Analysis and Design of Current-Reused CMOS VCOs, School of Computer Science and Engineering, February 2015.

Research adviser: T. Tsukahara

[tsuka-12:2014] Takuma Miura. Graduation Thesis: A Complex Quadrature Modulator using Doubled-LO-Frequency Switching Mixers, School of Computer Science and Engineering, February 2015.

Research adviser: T. Tsukahara

[tsuka-13:2014] Fumiki Moria. Graduation Thesis: Analysis and Design of Class-D CMOS Oscillators, School of Computer Science and Engineering, February 2015.

Research adviser: T. Tsukahara

[tsuka-14:2014] Kyosuke Arimura. Graduation Thesis: A Simplified Design Method of Microwave Class-E Power Amplifiers, School of Computer Science and Engineering, February 2015.

Research adviser: T. Tsukahara

[tsuka-15:2014] Jeewaka Dharmapriya. Master Thesis: Design Method for Fast Settling Phase Locked Loops, Graduate School of Computer Science and Engineering, February 2015.

Research adviser: T. Tsukahara

[tsuka-16:2014] Tomoko Nishiuchi. Master Thesis: Design of Wideband Receiver Front-End with Noise Cancelling in 0.18um CMOS Technology, Graduate School of Computer Science and Engineering, February 2015.

Research adviser: T. Tsukahara