Computer Logical Design Laboratory

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Tsuneo Tsukahara:

Software-Defined Radio Transceivers

Related to this topic, the following work was done in 2015.

A High-Precision Quadrature Modulator and High-Performance RF Front-End Circuits suitable for Multi-band Wireless Transceivers:

Recently the demand for wireless systems such as sensor networks has been rapidly growing. However, radio-wave resources are limited and invaluable especially in these days. Therefore, software-defied radios (SDRs) and cognitive radios, which is a principal application of SDR, can be the key to greatly improving frequency-spectrum efficiency. SDRs demand flexibility and reconfigurability in RF (Radio Frequency) circuits. Therefore, a spectrum-efficient wireless transceiver architecture is indispensable. In this research, we proposed a multi-band wireless transceiver using a high-precision complex quadrature modulator (HP-CQMOD) and a flexible-filtering receiver suitable for sensor networks. As the final goal of our research, we would like to establish a reconfigurable wireless communicator, whose frequency band can be changed according to communication conditions and/or regulations using reconfigurable RF and baseband processors and downloadable software. This is a kind of cognitive radios based on SDR (Software-Defined Radios). In recent years, multi-level modulations such as Quadrature Amplitude Modulation (QAM) are or will be used in Wireless LANs, digital TVs, and the 4th-generation cell-phones. So, very small modulation errors of QMOD are strongly demanded. In the 2015, we concentrated on circuit design of low-power HP-CQMODs, RF-band complex bandpass filters and linear power

amplifiers in the transmitter. Moreover, we devised a low-distortion rail-to-rail amplifier and rail-to-rail voltage-controlled oscillators.

RF/IF building blocks we designed have three features as follows:

1. Low-power high-precision complex quadrature modulators are newly developed, featuring a dual-LO switching quadrature mixer and an RF-band complex bandpass filter.
2. We proposed high-efficiency CMOS power amplifiers using a class-D mode.
3. Low-distortion and wideband rail-to-rail amplifiers.
4. Ril-to-rail voltage-controlled oscillators.

Yukihide Kohira:

We investigate *design automation methodology for LSI circuits*. Due to the increase of scales of LSI circuits and the decrease of time to market of LSI products, design automation systems are widely used in order to design LSI circuits. Since the performance of LSI depends on the used design automation systems, it is important to develop design automation methodology continuously in order to obtain good products.

Our research interests are design automation for clock synchronous framework and layout design. In 2015, we focused on following two topics.

General-synchronous Framework

In general-synchronous framework, a clock is distributed periodically to all registers but the clock is not necessarily distributed simultaneously. General-synchronous framework is expected to obtain LSI circuits with high performance and low power consumption. The target of this research is to establish a design automation system for general-synchronous framework. In 2015, we investigated implementation methods of circuits into FPGA in general-synchronous framework. In our experiments, circuits with higher performance were obtained by the proposed methods.

Placement of CMOS circuit in 1D-Layout Style

In layout design for LSI circuits, the layout area is minimized to reduce the fabrication cost and to increase the yield of LSI chips. In 1D-layout design, the width is shortened by sharing the diffusions and the height corresponds to the number of tracks. In 2015, we investigated an area minimization method for CMOS circuits using constraint programming in 1D-layout style.

Refereed academic journal

[tsuka-202-034-01:2015] M. Ugajin, Y. Kobayashi, and T. Tsukahara. High-Image-Rejection Wireless-Receiver Architecture with a 3-Phase Active RC Complex Filter. *IEICE Electronics Express*, 12(12):1–6, June 2015.

This paper proposes a high-image-rejection wireless-receiver architecture with a 3-phase active RC complex filter. The double conversion receiver, in cooperation with RF filter, rejects all image signals. In particular, the double conversion corrects the gain and phase mismatches of the adjacent image, and the image-rejection ratio of the adjacent image depends only on RC mismatches in the complex filter. Thus, the total image-rejection ratio of more than 60 dB can be expected for all the image signals.

Refereed proceedings of an academic conference

[tsuka-202-034-02:2015] T. Tsukahara, R. Ito, and K. Arimura. Complex Signal Processing Used in Modern RF Transceivers (Invited). In *2015 IEEE International Symposium on Radio Frequency Integration Technology (RFIT)*. IEEE, August 2015.

This paper first describes the evolution of RF transceiver architectures, especially focusing on state-of-the-art CMOS system-on-a-chip (SoC) implementation and software-defined radios (SDRs). Because, in these modern RF transceivers, complex signal processing is indispensable for digital modulation/demodulation and side-band or image-signal rejection in frequency conversion processes, fundamentals of complex signal processing are reviewed. Finally, we propose a high-precision complex quadrature modulator suitable for modern RF transmitters using multi-symbol quadrature amplitude modulation (QAM), which features the inherent correction mechanism of local-oscillator (LO) phase and amplitude errors. Especially, a newly proposed dual-LO-switching passive quadrature mixer plays an important role in the LO-phase error correction.

[tsuka-202-034-03:2015] T. Miyazaki, P. Li, S. Guo, J. Kitamichi, T. Hayashi, and T. Tsukahara. On-demand Customizable Wireless Sensor Network. In *The 6th International Conference on Ambient Systems, Networks and Technologies (ANT-2015)*, pages 302–309, June 2015.

In this paper, we propose a wireless sensor network (WSN) whose behavior can be dynamically customized by injecting programs or roles specified by the user.

To enable easy specification of the roles, a role-generation mechanism is also proposed. To realize the WSN, we introduce a reconfigurable wireless sensor node that has an ultra-low-power field-programmable gate array (FPGA) as well as a low-power microcontroller unit (MCU). By injecting several different roles into the sensor nodes, we confirmed that the behavior of the WSN can be changed on demand.

Unrefeered proceedings of an academic conference

[kohira-202-034-01:2015] H. Mashiko and Y. Kohira. Area Minimization Method for Layout of CMOS Circuits Using SAT-Solver. In *The 28th Workshop on Circuits and Systems*, pages 237–242, August 2015.

[kohira-202-034-02:2015] H. Mashiko, T. Oba, and Y. Kohira. Performance Improvement by Engineering Change Order in General-Synchronous Framework for Altera FPGA. In *IEICE Technical Report (VLD2015-137)*, volume 115, pages 149–154, March 2016.

[kohira-202-034-03:2015] H. Mashiko, T. Oba, and Y. Kohira. Implementation Flow of General-Synchronous Circuits into Altera FPGA. In *IEICE General Conference (A-6-1)*, volume A, page 75, March 2016.

[tsuka-202-034-04:2015] R. Ito and T. Tsukahara. High-Frequency Complex Bandpass Filter: Application to Quadrature Modulator. In *2015 Society Conference of IEEJ Electronics, Information and Systems*. IEE Japan, August 2015.

[tsuka-202-034-05:2015] T. Toshiaki, P. Li, S. Guo, T. Hayashi, J. Kitamichi, and T. Tsukahara. Implementation of Demand-Addressable Sensor Network Realizing Demand-Driven Wide-Area Sensing (Invited). In IEICE, editor, *IEICE Technical Report, Communication Systems*, 2015.

[tsuka-202-034-06:2015] K. Arimura and T. Tsukahara. Dual-LO Switching Mixers Featuring the LO-Phase-Error Compensation Mechanism. In *The Papers of Technical Meeting on Electronic Circuits*. IEE Japan, January 2016.

Research grants from scientific research funds and public organizations

[kohira-202-034-04:2015] Y. Kohira. Grant-in-Aid for Young Scientists (B) from Japan Society for the Promotion of Science (JSPS), 2014-2016.

[kohira-202-034-05:2015] A. Takahashi and Y. Kohira. Grants-in aid for Scientific Research (B) from Japan Society for the Promotion of Science (JSPS), 2013-2015.

[tsuka-202-034-07:2015] M. Ugajin and T. Tsukahara. Grants-in aid for Scientific Research (KAKENHI C) from JSPS, 2014-2016.

Academic society activities

[kohira-202-034-06:2015] Y. Kohira, 2015.

Committee Member, IEICE Technical Committee on VLSI Design Technologies (VLD)

[kohira-202-034-07:2015] Y. Kohira, July 2015.

Associate Editor, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Special Section on Design Methodologies for System on a Chip

[kohira-202-034-08:2015] Y. Kohira, August 2015.

Organizing Committee Member (Publication Chair), 28th Workshop on Circuits and Systems

[kohira-202-034-09:2015] Y. Kohira, December 2015.

Associate Editor, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Special Section on VLSI Design and CAD Algorithms

[kohira-202-034-10:2015] Y. Kohira, January 2016.

Technical Program Committee Member, 21st Asia and South Pacific Design Automation Conference (ASPDAC 2016), Design for Manufacturability Track

[tsuka-202-034-08:2015] T. Tsukahara, 2014-2016.

Chair of the IEEJ Investigating R/D Committee on New Application Fields and Supporting Technology of High-Frequency Integrated Circuits

Advisor for undergraduate research and graduate research

[kohira-202-034-11:2015] T. Oba. Master Thesis: Implementation of General-synchronous Circuits into Altera FPGA using Prescribed-Domain Clock Skew Scheduling, University of Aizu, March 2016.

Thesis Advisor: Y. Kohira

[kohira-202-034-12:2015] F. Sugiyama. Analytical Placement Using SPICE Simulator in LSI Circuits, University of Aizu, March 2016.

Thesis Advisor: Y. Kohira

[tsuka-202-034-09:2015] Shun Kato. Graduation Thesis: Analysis and Design of VCOs using a Rail-to-Rail CMOS Differential Amplifier, Computer Science and Engineering, March 2016.

[tsuka-202-034-10:2015] Tomoki Shoji. Graduation Thesis: A Limiting Amplifier using a Rail-to-Rail CMOS Differential Amplifier, Computer Science and Engineering, March 2016.

[tsuka-202-034-11:2015] Chiro Ikoma. Graduation Thesis: Analysis and Design of CMOS Cherry-Hooper Amplifiers, Computer Science and Engineering, March 2016.

[tsuka-202-034-12:2015] Yuta Shimizu. Graduation Thesis: Analysis and Design of a CMOS Power Amplifier, Computer Science and Engineering, March 2016.

[tsuka-202-034-13:2015] Ryo Ito. Master Thesis: Design of Radio Frequency (RF) Complex Bandpass Filter, Graduate School of Computer Science and Engineering, March 2016.

Others

[tsuka-202-034-14:2015] T. Tsukahara. Fundamentals of Fractional-N Synthesizer: Master Course Lecture, Keio University, December 2015.