Distributed Pararell Processing Laboratory

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Refereed academic journal

[nakasato-204-005-01:2015] Ataru Tanikawa, Naohito Nakasato, Yushi Sato, Ken'ichi Nomoto, Keiichi Maeda, and Izumi Hachisu. Hydrodynamical evolution of merging carbon-oxygen white dwarfs: their pre-supernova structure and observational counterparts. *Astrophysical Journal*, 807(1):40, 2015.

We perform smoothed particle hydrodynamics simulations for merging binary carbon-oxygen (CO) WDs with masses of 1.1 and 1.0 Mo, until the merger remnant reaches a dynamically steady state. Using these results, we assess whether the binary could induce a thermonuclear explosion, and whether the explosion could be observed as a type Ia supernova (SN Ia). We investigate three explosion mechanisms: a helium-ignition following the dynamical merger (helium-ignited violent merger model), a carbon-ignition (carbon-ignited violent merger model), and an explosion following the formation of the Chandrasekhar mass WD (Chandrasekhar mass model).

[nakasato-204-005-02:2015] Yushi Sato, Naohito Nakasato, Ataru Tanikawa, Ken'ichi Nomoto, Keiichi Maeda, and Izumi Hachisu. A systematic study of carbon-oxygen white dwarf mergers: mass combinations for Type Ia supernovae. *Astrophysical Journal*, 807(1):105, 2015.

Mergers of two carbon-oxygen (CO) white dwarfs (WDs) have been considered as progenitors of Type Ia supernovae (SNe Ia). Based on smoothed particle hydrodynamics (SPH) simulations, previous studies claimed that mergers of CO WDs lead to an SN Ia explosion either in the dynamical merger phase or stationary rotating merger remnant phase. However, the mass range of CO WDs that lead to an SN Ia has not been clearly identified yet. In the present work, we perform systematic SPH merger simulations for the WD masses ranging from 0.5 Mo to 1.1 Mo with higher resolutions than the previous systematic surveys and examine whether or not carbon burning occurs dynamically or quiescently in each phase.

Refereed proceedings of an academic conference

[nakasato-204-005-03:2015] Kentaro Sano, Fumiya Kono adn Naohito Nakasato, Alexander Vazhenin, and Stanislav Sedukhin. Stream Computation of Shallow Water Equation Solver for FPGA-based 1D Tsunami Sim-

ulation. In *ACM SIGARCH Computer Architecture News - HEART '15*, volume 43, pages 82–87, 2015.

MOST (Method Of Splitting Tsunami) is widely used to solve shallow water equations (SWEs) for forecasting tsunami generated by an earthquake. Toward development of a power-efficient and high-performance computing system for 2D tsunami simulation, we conduct feasibility study on stream computation of 1D SWE solver with FPGA.We analyze an original code and design a stream algorithm with techniques of kernel fusion, shift buffering for streamed stencil-data access, and cascading processing elements for a longer pipeline. We implement a deep pipeline with at most 744 stages of 4 SPEs on 28 nm Stratix V FPGA, which achieves 82.4 GFlop/s at 200 MHz.

[nakasato-204-005-04:2015] Hiroshi Daisaka, Naohito Nakasato, Tadashi Ishikawa, and Fukuko Yuasa. Application of GRAPE9-MPX for high precision calculation in particle physics and performance results. In *Procedia Computer Science*, volume 51, pages 1323–1332, 2015.

There are scientific applications which require calculations with high precision such as Feynman loop integrals and orbital integrations. These calculations also need to be accelerated. We have been developing dedicated accelerator systems which consist of processing elements (PE) for high precision arithmetic operations and a programing interface. GRAPE9-MPX is our latest system with multiple Field Programmable Gate Array (FPGA) boards on which our developed PEs are implemented. We present the performance results for GRAPE9-MPX extended to have up to 16 FPGA boards for quadruple, hexuple, and octuple precision calculation. The achieved performance for a Feynman loop integral with 12 FPGA boards is 26.5 Gflops for quadruple precision, 13.2 Gflops for hexuple precision, and 6.36 Gflops for octuple precision. We show that our hardware implementation is 80 - 200 times faster than software implementations. We also give analysis of the performance results.

[nakasato-204-005-05:2015] Yuki Murakami, Naohito Nakasato, and Stanislav Sedukhin. FPGA implementation of a SIMD-based array processor with torus interconnect. In *International Conference on Field Programmable Technology (FPT) 2015*, pages 1–4, 2015.

Matrix computations are a fundamental tool in scientific and engineering applications. Among many such applications, Convolutional Neural Net-

works (CNN) that can be effectively computed by matrix-matrix multiplications are being popular and an efficient implementation of CNN is highly important. In this study, we have designed an parallel processor for the matrix computations using torus interconnect topology, and we implemented Cannon's algorithm for matrix-matrix multiply-add. We have evaluated the scalability of the proposed processor on a reconfigurable FPGA platform. More precisely, the designed processor with 8x8 functional units with 16 bit floating-point multiply-add unit was evaluated on Cyclone IV FPGA chip, with performance of 27 GFlops. We also implemented CNN calculations on our processor. We compared the matrix based approach and our proposed method. As a result, our method is 25 times faster than the matrix based approach if the processor has 8x8 functional units, image size is 32x32 and filter size is 5x5.

Advisor for undergraduate research and graduate research

[nakasato-204-005-06:2015] Yuki Murakami. Master Thesis: FPGA Implementation of a SIMD-Based Array Processor with Torus Interconnect, University of Aizu, 2016.

Thesis Advisor: N. Nakasato

[nakasato-204-005-07:2015] Masaya Kobayashi. Graduation Thesis: Evaluation of Artificial Neural Networks for Solving Differential Equations Using Chainer, University of Aizu, 2016.

Thesis Advisor: N. Nakasato