Embedded Systems Laboratory

Junji Kitamichi
Professor

Yoichi Tomioka
Associate Professor

The Embedded Systems Laboratory was established in July, 2013. In April, 2015, Prof. Tomioka joined in the Embedded Systems Laboratory. Embedded systems are products which computers are embedded, and the research region of the embedded systems is very wide, such as software, hardware, and middle-ware, from theory to application, calculation performance, power consumption, safety, and development methods. We are researching the following themes out of many research topics about embedded systems.

1. Safety Embedded System
(a) Formal Approach for Circuits Design and Systems Design
(b) Design Method of Safety Systems
2. Hardware acceleration of Heuristic Approaches for Combinatorial Optimization Problems
3. Image Processing and its Power-efficient Accelerator
(a) Video Analysis and Privacy Protection for Surveillance Camera
(b) Deep learning hardware
(c) Application of Image recognition to Lithography Hotspot Detection
(d) Image forensics

Members of the Embedded Systems Laboratory

Prof. Junji Kitamichi:

He received the B.S. and Ph.D degrees in information and computer sciences from Osaka University, Japan, in 1988 and 1999, respectively. In 1991, he joined the Department of Information and Computer Sciences at Osaka University, Japan, as a research associate. From 1999 to 2002, he was with Cybermedia Center at

Osaka University, where he was assistant professor. In 2002, he joined School of Computer Science and Engineering, the University of Aizu, Japan. He was a professor at the University of Aizu from 2013. His research interests include formal methods for VLSI design, dynamically reconfigurable systems, formal design and verification of safety systems, heuristics and parallel algorithms for combinatorial optimization problems.

Prof. Yoichi Tomioka: He received his B.E., M.E., and D.E. degrees from Tokyo Institute of Technology, Tokyo, Japan,in 2005, 2006, and 2009, respectively. He was a research associate at Tokyo Institute of Technology till 2009. He was an assistant professor in the Division of Advanced Electrical and Electronics Engineering at Tokyo University of Agriculture and Technology till 2015. Since 2015, he has been an associate professor in School of Computer Science and Engineering at the University of Aizu. His research interests include image processing, hardware acceleration, high performance computing, electrical design automation, and combinational algorithms.

Students :

B3:Yuji Matumoto, Sho Ikeda, Dai Funayama, Shu Takenoshita, Yuma Otsu, Yoshifumi Kato, Yusuke Sekiguchi

B4:Souichirou Endou, Hiroki Saito, Kanji Kobayashi, Ryohei Yamauchi, Hiroyuki Niida

Refereed academic journal

[ytomioka-208-033-01:2015] Hitoshi Kitazawa Tetsuya Okuda, Yoichi Tomioka. Robust Moving Object Extraction and Tracking Method based on Matching Position Constraints. *IEICE Trans. on Information and Systems*, E98-D(8):1571–1579, 2015.

Object extraction and tracking in a video image is basic technology for many applications, such as video surveillance and robot vision. Many moving object extraction and tracking methods have been proposed. However, they fail when the scenes include illumination change or light reflection. For tracking the moving object robustly, we should consider not only the RGB values of input images but also the shape information of the objects. If the objects shapes do not change suddenly, matching positions on the cost matrix of exclusive block matching are located nearly on a line. We propose a method for obtaining the correspondence of feature points by imposing a matching position constraint induced by the shape constancy. We demonstrate experimentally that the proposed method achieves robust tracking in various environments.

Refereed proceedings of an academic conference

[kitamiti-208-033-01:2015] Yoichi Tomioka Hiroki Saito and Junji Kitamichi. Proposing a Highly Reliable Real-Time Operating System for a Processor with a Fault Self-detecting Mechanism. In *13th International Conference on Embedded Software and Systems*, 2016.

Presently, failures and malfunctions of embedded systems can cause serious problems. A highly safe and reliable system requires the ability to deal with failure and malfunction. Furthermore, the sophistication and complexity of real-time systems are increasing with the evolution of technology. We propose a highly reliable real-time operating system (RTOS). The proposed RTOS has a fault detection function for the MicroController Unit (MCU) for real-time applications. This paper reports on the development of an extended function and a fault detection function for RTOS for high-reliability systems. A self-test function of a system and a function that improves the reliability of the MCU are offered. Application Programming Interfaces (APIs) have been developed for fault detection. By developing and running application programs on the system with the developed RTOS, we confirm that the developed RTOS startups and switches multi-tasks and executes cyclic tasks by external timer

interrupts. The fault detection function is evaluated using developed application programs. By evaluating the results, we confirm the reliability of the system by the self-test function.

[ytomioka-208-033-02:2015] Ning Li, Shunpei Takaki, Yoichi Tomioka, and Hitoshi Kitazawa. A MULTISTAGE DATAFLOW IMPLEMENTATION OF A DEEP CONVOLUTIONAL NEURAL NETWORK BASED ON FPGA FOR HIGH-SPEED OBJECT RECOGNITION. In *Proc of IEEE SOUTHWEST SYMPOSIUM ON IMAGE ANALYSIS AND INTERPRETATION*, March 2016.

Deep Neural Networks (DNNs) have progressed significantly in recent years. Novel DNN methods allow tasks such as image and speech recognition to be conducted easily and efficiently, compared with previous methods that needed to search for valid feature values or algorithms. However, DNN computations typically consume a significant amount of time and high-performance computing resources. To facilitate high-speed object recognition, this article introduces a Deep Convolutional Neural Network (DCNN) accelerator based on a field-programmable gate array (FPGA). Our hardware takes full advantage of the characteristics of convolutional calculation; this allowed us to implement all DCNN layers, from image input to classification, in a single chip. In particular, the dateflow from input to classification is uninterrupted and paralleled. As a result, our implementation achieved a speed of 409.62 gigaoperations per second (GOPS), which is approximately twice as fast as the latest reported result. Furthermore, we used the same architecture to implement a Recurrent Convolutional Neural Network (RCNN), which can, in theory, provide better recognition accuracy.

[ytomioka-208-033-03:2015] Yutaro Ishigaki, Yoichi Tomioka, Tsugumichi Shibata, and Hitoshi Kitazawa. An FPGA Implementation of 3D Numerical Simulations on a 2D SIMD Array Processor. In *Proc. of IEEE International Symposium on Circuits and Systems*, pages 938–941, May 2015.

In this paper, we propose an FPGA-based accelerator for 3D numerical simulations and focus on acceleration of the 3D FDTD method. This accelerator consists of a 2D SIMD array processor, and it can execute 3D parallel computing with little data transfer overhead by applying virtual processing-elements cuboid (VPEC) with synchronous shift data transfer. We demonstrate that the experimental hardware implemented on an Altera Stratix V FPGA (5SGSMD5K2F40C2N) is 3.1 times faster than parallel computing on

the NVIDIA Tesla C2075, and it reaches a 94.57% operating rate of the calculation units. The proposed accelerator is suitable for multi-chip composition.

Unrefeered proceedings of an academic conference

[kitamiti-208-033-02:2015] H. Saito and J. Kitamichi. Proposal of a Real Time Operating System for a Safety Processor. In IPSJ, editor, *The 78th National Convention of IPSJ*, pages 3G–04. IPSJ, March 2016.

We propose a highly reliable real-time operating system (RTOS). The proposed RTOS has a fault detection function for the MicroController Unit (MCU) for real-time applications. This paper reports on the development of an extended function and a fault detection function for RTOS for high-reliability systems. A self-test function of a system and a function that improves the reliability of the MCU are offered. Application Programming Interfaces (APIs) have been developed for fault detection. By developing and running application programs on the system with the developed RTOS, we confirm that the developed RTOS startups and switches multi-tasks and executes cyclic tasks by external timer interrupts. The fault detection function is evaluated using developed application programs. By evaluating the results, we confirm the reliability of the system by the self-test function.

[kitamiti-208-033-03:2015] IPA(Information technology Promotion Agency) SEC(Software Reliability Enhancement Center) Software Reliability Enhancement Promotion Committee System Fault Diagnosis WG. System Fault Diagnosis Methods for Large and Complicated Embedded Systems / Proposal of Post hoc V&V by Model Base Approach. In IPA, editor, *IPA Report*. IPA, IPA, March 2017.

[kitamiti-208-033-04:2015] Youichi Tomioka Yuji Matumoto and Junji Kitamichi. A Hardware Acceleration of Template Matching using FPGA and MPU. In *IEICE, Tech, Rep.*

, vol. 116, no. 417, RECONF2016-51, pages 1 –6, 2016.

[ytomioka-208-033-04:2015] Syota Saito, Yoichi Tomioka, and Hitoshi Kitazawa. Accuracy Evaluation Method forCamera Identification using Pair of Clustered PRNU Noise. In *Proc. of ITE Annual Convention*, August 2015.

A camera identification method using pair of clustered PRNU noise has been proposed. However, the accuracy of this method has not been analyzed precisely yet. In this paper, by clarifying the mathmatical model of the mismatch probability of cluster-pair, we evaluate the accuracy based on probability calculation.

[ytomioka-208-033-05:2015] Atsuki Yasue, Yoichi Tomioka, and Hitoshi Kitazawa. Characteristics on Scanner Identification using Clustered PRNU Noises. In *Proc. of ITE Annual Convention*, August 2015.

A scanner identification method using clustered PRNU noise has been presented. This study aims to identify the scanner which was used to scan query images. It can be applicaed to detect the scanner which has been used to upload comics and magazines illegally. This paper reports the effects of secular changes, background color of scanned paper, and a different scanner of the same model on scanner identification.

[ytomioka-208-033-06:2015] Ning Li, Shunpei Takaki, Yoichi Tomioka, and Hitoshi Kitazawa. An Implementation of DCNN with Dataflow Architecture for High Speed Moving Object Recognition. In *Proc. of National Convention of IPSJ*, pages 1–115–116, March 2016.

This article introduces a Deep Convolutional Neural Network (DCNN) accelerator based on a field-programmable gate array (FPGA). In addition to the results presented in SSIAI2016, we propose a novel convolution circuit. It can save the resouce usage by sharing it with multiple layers.

[ytomioka-208-033-07:2015] Yoichi TOMIOKA and Tetsuaki MATSUNAWA.

Lithography Hotspot Detection using Histogram of Oriented Light Propagation. In *IEICE Technical Report*, volume VLD2015-136, pages 143–148, March 2016.

In recent semiconductor manufacturing process, it is essential to detect and to remove lithography hotspots, which induce printability issues. The machine learning based hotspot detection has recently been received attractive attentions. It is important to use appropriate features to capture essential characteristics of hotspots to precisely detect unknown hotspots that are not used in training. In this paper, we propose a novel layout feature based on the propagation of light passing through a photomask. Moreover, we report methods to construct a reliable hotspot detector that can reduce false alarms which are similar to hotspots.

Research grants from scientific research funds and public organizations

[ytomioka-208-033-08:2015] Yoichi Tomioka. Establishment of methods for robustly identifying source devices of digital images, JSPS Grant-in-Aid for Scientific Research (C), 2014–2016.

Academic society activities

[kitamiti-208-033-05:2015] Kitamichi J., 2014.

Member. IEEE

[kitamiti-208-033-06:2015] Kitamichi J., 2014.

Member, IPSJ

[kitamiti-208-033-07:2015] Kitamichi J., 2014.

Member and Editorial Committee Member, IEICE. Steering Comittee Member, Tohoku Branch, IEICE

[kitamiti-208-033-08:2015] Kitamichi J., 2014-2015.

Councilor, IEICE

[kitamiti-208-033-09:2015] Kitamichi J., 2014.

System Fault Diagnosis WG Member,Software Reliability Enhancement Center (SEC) , IPA

[kitamiti-208-033-10:2015] Kitamichi J., 2014-2015.

Editor of Editorial Committee of the IEICE Transactions on Special Section onFormal Approach

[ytomioka-208-033-09:2015] Yoichi Tomioka, 2015.

IEICE Technical Committe Member of Reconfigurable systems

Advisor for undergraduate research and graduate research

[kitamiti-208-033-11:2015] Kobayashi Kanji. Graduation Thesis: Improvement of processing speed of Neural Network Algorithm for Channel A ssignment Problem using SIMD Co-processor, University of Aizu, 2015.

Thesis Advisor: J. Kitamichi

[kitamiti-208-033-12:2015] Hiroyuki Niida. Graduation Thesis:An Evaluation of Partial Reconfiguration Function of an Altera's FPGA, University of Aizu, 2015.

Thesis Advisor: J. Kitamichi

[kitamiti-208-033-13:2015] Soichiro Endo. Graduation Thesis:Modeling and Verification of Embedded Systems using Formal Verification T ool LTSA, University of Aizu, 2015.

Thesis Advisor: J. Kitamichi

[kitamiti-208-033-14:2015] Hiroki Saito. Graduation Thesis:A Development of High Reliable Real Time Operating System for a Fault Sel f-detection Processor, University of Aizu, 2015.

Thesis Advisor: J. Kitamichi