

Computer Logical Design Laboratory



Tsuneo Tsukahara
Professor



Yukihide Kohira
Senior Associate Professor



Yu Nakajima
Research Assistant

Tsuneo Tsukahara:

Software-Defined Radio Transceivers

Related to this topic, the following work was done in 2016.

A High-Precision Quadrature Modulator and High-Performance RF Front-End Circuits suitable for Multi-band Wireless Transceivers:

Recently the demand for wireless systems such as sensor networks has been rapidly growing. However, radio-wave resources are limited and invaluable especially in these days. Therefore, software-defined radios (SDRs) and cognitive radios, which is a principal application of SDR, can be the key to greatly improving frequency-spectrum efficiency. SDRs demand flexibility and reconfigurability in RF (Radio Frequency) circuits. Therefore, a spectrum-efficient wireless transceiver architecture is indispensable. In this research, we proposed a multi-band wireless transceiver using a high-precision complex quadrature modulator (HP-CQMOD) and a flexible-filtering receiver suitable for sensor networks. As the final goal of our research, we would like to establish a reconfigurable wireless communicator, whose frequency band can be changed according to communication conditions and/or regulations using reconfigurable RF and baseband processors and downloadable software. This is a kind of cognitive radios based on SDR (Software-Defined Radios). In recent years, multi-level modulations such as Quadrature Amplitude Modulation (QAM) are or will be used in Wireless LANs, digital TVs, and the 4th-generation cell-phones. So, very small modulation errors of QMOD are strongly demanded. In the 2016, we concentrated on circuit design of low-power HP-CQMODs, RF-band complex bandpass filters and linear power

Division of Computer Engineering

amplifiers in the transmitter. Moreover, we devised a low-distortion rail-to-rail amplifier and rail-to-rail voltage-controlled oscillators.

RF/IF building blocks we designed have three features as follows:

1. Low-power high-precision complex quadrature modulators are newly developed, featuring a dual-LO switching quadrature mixer and an RF-band complex bandpass filter. Regarding the dual-LO switching quadrature modulator, we made breadboard experiments using commercially available ICs for analog switches and OP amplifiers and confirmed the usefulness of LO-phase error compensation mechanism.
2. Low-distortion and wideband rail-to-rail amplifiers combining with the Cherry-Hooper architecture.
3. Rail-to-rail voltage-controlled oscillators.

Yukihide Kohira:

We investigate *design automation methodology for LSI circuits*. Due to the increase of scales of LSI circuits and the decrease of time to market of LSI products, design automation systems are widely used in order to design LSI circuits. Since the performance of LSI depends on the used design automation systems, it is important to develop design automation methodology continuously in order to obtain good products.

Our research interests are design automation for clock synchronous framework and layout design. In 2016, we focused on following four topics.

General-synchronous Framework

In general-synchronous framework, a clock is distributed periodically to all registers but the clock is not necessarily distributed simultaneously. General-synchronous framework is expected to obtain LSI circuits with high performance and low power consumption. In 2016, we investigated an implementation method of circuits into FPGA in general-synchronous framework. Moreover, we published a refereed thesis on technology mapping in which assigns a cell in cell libraries to each gate in an academic journal.

Deskew

In resent LSI circuits, process variations increase significantly because of the progress of the process technology. The process variations significantly cause delay variations and delay variations affect the performance and the yield of

VLSI chips. If the circuit cannot work at the testing process after the fabrication of LSI chips, the circuit can be recovered by deskew in which delay of the programmable delay elements is adjusted. In 2016, we investigated delay turning methods to improve the yield and to reduce the power consumption and published theses in an international conference and a domestic conference.

Placement of CMOS circuit in 1D-Layout Style

In layout design for LSI circuits, the layout area is minimized to reduce the fabrication cost and to increase the yield of LSI chips. In 1D-layout design, the width is shortened by sharing the diffusions and the height corresponds to the number of tracks. In 2016, we published refereed theses on area minimization methods for CMOS circuits using constraint programming in 1D-layout style in an international conference and an academic journal.

Lithography

Multiple patterning technique enables us to fabricate small features without using advanced technologies such as extreme ultra violet (EUV) lithography. Triple patterning lithography is one of the most promising techniques in 14 nm logic node and beyond. Two types of triple patterning technologies are often discussed in literature. In LELELE, litho-etch process is repeated three times. In LELECUT, the third mask called cut process removes a part of a fabricated pattern. It is used to improve the quality of fabricated patterns as well as to enhance the flexibility of layout. In 2016, we published theses on a fast layout decomposition algorithm in LELELE and LELECUT by using positive semidefinite relaxation in an international conference and an academic journal.

Summary of Achievement

Refereed academic journal

- [kohira-202-034-01:2016] Y. Kohira, C. Kodama, T. Matsui, A. Takahashi, S. Nojima, and S. Tanaka. Yield-aware mask assignment by positive semidefinite relaxation in triple patterning using cut process. *J. Micro/Nanolith. MEMS MOEMS*, 15(2), 2016.

LELECUT type triple patterning lithography is one of the most promising techniques in 14 nm logic node and beyond. To prevent yield loss caused by overlay error, LELECUT mask assignment, which is tolerant to overlay error, is desired. We propose a method that obtains a LELECUT assignment that is tolerant to overlay error. The proposed method uses positive semidefinite relaxation and randomized rounding technique. In our method, the cost function that takes the length of boundary of features determined by the cut mask into account is introduced.

- [kohira-202-034-02:2016] J. Kawaguchi, H. Mashiko, and Y. Kohira. Technology Mapping Method using Integer Linear Programming for Low Power Consumption and High Performance in General-Synchronous Framework. *IEICE Trans. Fundamentals*, E99-A(7):1366–1373, 2016.

In general-synchronous framework, in which the clock is distributed periodically to each register but not necessarily simultaneously, circuit performance is expected to be improved compared to complete-synchronous framework, in which the clock is distributed periodically and simultaneously to each register. To improve the circuit performance more, logic synthesis for general-synchronous framework is required. In this paper, under the assumption that any clock schedule is realized by an ideal clock distribution circuit, when two or more cell libraries are available, a technology mapping method which assigns a cell to each gate in the given logic circuit by using integer linear programming is proposed. In experiments, we show the effectiveness of the proposed technology mapping method.

- [kohira-202-034-03:2016] H. Mashiko and Y. Kohira. Area Minimization Method for CMOS Circuits Using Constraint Programming in 1D Layout Style. *IEICE Trans. Fundamentals (Japanese Edition)*, J100-A(1):79–91, 2017.

In layout design for LSI circuits, the layout area is minimized to reduce the fabrication cost and to increase the yield of LSI chips. In 1D layout style of transistor level CMOS circuits, where layout patterns do not bend, the width is

shortened by sharing the diffusions and the height corresponds to the number of tracks. The existing layout methods minimize the number of tracks under the condition that the number of shared diffusions is maximized. However, the layout with minimum area can be obtained by minimizing the number of tracks without maximizing the number of shared diffusions, since the height is shorter than the width in general. In this paper, a method which solves the CMOS layout area minimization problem in a constraint programming is proposed. In the proposed method, under the assumption that a given netlist of the CMOS circuit is not changed, the number of shared diffusions is maximized with the restriction of the number of tracks. The effectiveness of the proposed method is confirmed in the experiments.

[tsuka-202-034-01:2016] T. Miyazaki, N. Suematsu, D. Baba, P. Li, S. Guo, J. Kitamichi, H. Hayashi, and T. Tsukahara. Demand-Addressable Sensor Network: Toward Large-Scale Active Information Acquisition. *IEEE Sensor Journal*, 16(20):pp. 7421–7432, October 2016.

A new type of sensor network called the demand-addressable sensor network (DASN) is proposed in this paper. The DASN actively acquires the desired information by addressing user demands and delivers the information to appropriate destinations. This is in contrast to the conventional sensor networks that simply send sensed data to users. The DASN is useful for finding the desired information in a short duration of time from a large amount of sensed data generated by a large-scale sensor network. The DASN is constructed with a demand-addressable network that integrates many on-demand reconfigurable wireless sensor networks (ODRWSN) and other existing information and communications technology systems or services, such as Google Maps and Twitter. In addition to the demand-addressing mechanism, the demand-addressable network has an in-network data combining or mashup mechanism. In this paper, the concept underlying the DASN, its architecture and implementation, and experimental results are presented.

Refereed proceedings of an academic conference

[kohira-202-034-04:2016] H. Mashiko and Y. Kohira. Area Minimization Method for CMOS Circuits Using Constraint Programming in 1D-Layout Style. In *2016 International Symposium on VLSI Design, Automation and Test (2016 VLSI-DAT)*. IEEE, April 2016.

Summary of Achievement

In layout design for LSI circuits, the layout area is minimized to reduce the fabrication cost and to increase the yield of LSI chips. In 1D-layout design, the width is shortened by sharing the diffusions and the height corresponds to the number of tracks. In this paper, an area minimization method for CMOS circuits using constraint programming in 1D-layout style is proposed. The experimental results show the effectiveness of the proposed method.

[kohira-202-034-05:2016] H. Mashiko and Y. Kohira. Yield and Power Improvement Method by Post-Silicon Delay Tuning and Technology Mapping. In *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2016)*, pages 366–369. IEEE, October 2016.

To recover the timing violations due to the delay variations after fabrication, delay tuning is promising. Delay tuning inserts programmable delay elements (PDEs) to circuits before fabrication and tunes their delays to recover the timing violations after fabrication. However, the yield of the circuits obtained by existing delay tuning methods is not improved enough and their power consumptions become high. Besides, technology mapping which assigns a cell in some cell libraries to each gate to minimize the clock period and the power consumption has been proposed. In this paper, a design method applying delay tuning and technology mapping for high yield improvement and low power consumption is proposed. The experimental results show the effectiveness of the proposed method.

[kohira-202-034-06:2016] Y. Kohira, A. Takahashi, T. Matsui, C. Kodama, S. Nojima, and S. Tanaka. Manufacturability-Aware Mask Assignment in Multiple Patterning Lithography. In *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2016)*, pages 538–541. IEEE, October 2016.

Due to the progress of the process technology, multiple patterning lithography (MPL) is one of the most promising techniques in the 22 nm logic node and beyond. In MPL, features are iteratively formed onto a wafer by exposures. Mask misalignment is caused during MPL process and it reduces the yield of the produced LSI in MPL. To prevent yield loss caused by the mask misalignment, mask assignment methods that take the manufacturability into consideration are desired. Recent mask assignment techniques in MPL are introduced.

Unrefereed proceedings of an academic conference

- [kohira-202-034-07:2016] M. Terada, H. Mashiko, and Y. Kohira. Implementation Flow of General-Synchronous Circuits from RTL Representation for Xilinx FPGA. In *IEICE Technical Report (VLD2016-48)*, volume 116, pages 25–30, November 2016.
- [kohira-202-034-08:2016] H. Mashiko and Y. Kohira. Post-Silicon Delay Tuning Method for Power Reduction considering Yield Improvement. In *IEICE Technical Report (VLD2016-104)*, volume 116, pages 13–18, March 2017.
- [tsuka-202-034-02:2016] K. Arimura and T. Tsukahara. Design and Analysis of a Dual-LO Switching Mixer for High-Precision Quadrature Modulators. In *The Papers of Technical Meeting on Electronic Circuits, IEE Japan*, number ECT-17-30, March 2017.

Research grants from scientific research funds and public organizations

- [kohira-202-034-09:2016] Y. Kohira. Grant-in-Aid for Young Scientists (B) from Japan Society for the Promotion of Science (JSPS), 2014-2016.
- [tsuka-202-034-03:2016] M. Ugajin and T. Tsukahara. Grants-in aid for Scientific Research (KAKENHI C) from JSPS, 2014-2016.

Academic society activities

- [kohira-202-034-10:2016] Y. Kohira, 2016.
Committee Member, IEICE Technical Committee on VLSI Design Technologies (VLD)
- [kohira-202-034-11:2016] Y. Kohira, 2016.
Associate Editor, IEICE Trans. Fundamentals
- [kohira-202-034-12:2016] Y. Kohira, July 2016.
Guest Editor, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Special Section on Design Methodologies for System on a Chip

Summary of Achievement

[kohira-202-034-13:2016] Y. Kohira, October 2016.

TPC Subcommittee Chair, Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2016), Physical subcommittee

[kohira-202-034-14:2016] Y. Kohira, December 2016.

Associate Editor, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Special Section on VLSI Design and CAD Algorithms

[kohira-202-034-15:2016] Y. Kohira, January 2017.

Technical Program Committee Member, 22nd Asia and South Pacific Design Automation Conference (ASPDAC 2017), Design for Manufacturability track

[kohira-202-034-16:2016] Y. Kohira, January 2017.

Liaison with ASPDAC 2017 Organizing Committee and Confirmed Committee Member, ACM SIGDA Student Research Forum at ASPDAC 2017

[tsuka-202-034-04:2016] T. Tsukahara, 2014-2016.

Chair of the IEEJ Investigating R/D Committee on New Application Fields and Supporting Technology of High-Frequency Integrated Circuits

Advisor for undergraduate research and graduate research

[kohira-202-034-17:2016] Y. Mashiko. Doctoral Thesis: Digital LSI Design Methods Considering Process Variations in Advanced Technology Nodes, University of Aizu, March 2017.

Thesis Advisor: Y. Kohira

[kohira-202-034-18:2016] M. Terada. Master Thesis: Implementation Flow in General-Synchronous Framework using Engineering Change Order for Xilinx FPGA, University of Aizu, March 2017.

Thesis Advisor: Y. Kohira

[kohira-202-034-19:2016] M. Aoki. Graduation Thesis: Design Method using Multiple Supply Voltages for Low Power in General-Synchronous Framework, University of Aizu, March 2017.

Thesis Advisor: Y. Kohira

[tsuka-202-034-05:2016] Emiri Takada. Graduation Thesis: Analysis and Design of a Wideband-IF Receiver using MOS Passive Mixers, School of Computer and Science Engineering, UoA, Feb. 2017.

Thesis Advisor: T. Tsukahara

[tsuka-202-034-06:2016] Atsushi Takegahara. Graduation Thesis: Design of a Quadrature LC-Oscillator using Rail-to-Rail CMOS Differential Amplifiers, School of Computer and Science Engineering, UoA, Feb. 2017.

Thesis Advisor: T. Tsukahara

[tsuka-202-034-07:2016] Yuji Masubuchi. Graduation Thesis: Design of a Class-C LC-Oscillator with an Adaptive Bias Circuit, School of Computer and Science Engineering, UoA, Feb. 2017.

Thesis Advisor: T. Tsukahara

[tsuka-202-034-08:2016] Minami Hatanaka. Graduation Thesis: A Differential CMOS Cherry-Hooper Amplifier and Its Applications to Limiting Amplifiers and Filters, School of Computer and Science Engineering, UoA, Feb. 2017.

Thesis Advisor: T. Tsukahara

[tsuka-202-034-09:2016] Satoshi Takara. Graduation Thesis: Analysis and Experimental Works of a 2.4-GHz-Bnad High-Precision Complex Quadrature Modulator (HP-CQMOD) LSI, School of Computer and Science Engineering, UoA, Feb. 2017.

Thesis Advisor: T. Tsukahara

[tsuka-202-034-10:2016] Kyosuke Arimura. Master Thesis: Design and Analysis of a Dual-LO Switching Quadrature Mixer for High-Precision Quadrature Modulators, Graduate School of Computer and Science Engineering, UoA, Feb. 2017.

Thesis Advisor: T. Tsukahara

Others

[tsuka-202-034-11:2016] T. Tsukahara. Fundamentals of Fractional-N Synthesizer, Jan. 2017.

Master Course Lecture, Keio University

Summary of Achievement

Contributions related to regional education

[tsuka-202-034-12:2016] Chair of the Aizu-Area Education and Science Foundation Evaluation Committee