Embedded Systems Laboratory

Junji Kitamichi
Professor

Yoichi Tomioka
Associate Professor

The Embedded Systems Laboratory was established in July, 2013. In April, 2015, Prof. Tomioka joined in the Embedded Systems Laboratory. Embedded systems are products which computers are embedded, and the research region of the embedded systems is very wide, such as software, hardware, and middle-ware, from theory to application, calculation performance, power consumption, safety, and development methods. We are researching the following themes out of many research topics about embedded systems.

1. Safety Embedded System
(a) Formal Approach for Circuits Design and Systems Design
(b) Design Method of Safety Systems
2. Hardware acceleration of Heuristic Approaches for Combinatorial Optimization Problems
3. Image Processing and its Power-efficient Accelerator
(a) Video Analysis and Privacy Protection for Surveillance Camera
(b) Deep learning hardware
(c) Application of Image recognition to Lithography Hotspot Detection
(d) Image forensics

Members of the Embedded Systems Laboratory

Prof. Junji Kitamichi:

He received the B.S. and Ph.D degrees in information and computer sciences from Osaka University, Japan, in 1988 and 1999, respectively. In 1991, he joined the Department of Information and Computer Sciences at Osaka University, Japan, as a research associate. From 1999 to 2002, he was with Cybermedia Center at

Osaka University, where he was assistant professor. In 2002, he joined School of Computer Science and Engineering, the University of Aizu, Japan. He was a professor at the University of Aizu from 2013. His research interests include formal methods for VLSI design, dynamically reconfigurable systems, formal design and verification of safety systems, heuristics and parallel algorithms for combinatorial optimization problems.

Prof. Yoichi Tomioka: He received his B.E., M.E., and D.E. degrees from Tokyo Institute of Technology, Tokyo, Japan,in 2005, 2006, and 2009, respectively. He was a research associate at Tokyo Institute of Technology till 2009. He was an assistant professor in the Division of Advanced Electrical and Electronics Engineering at Tokyo University of Agriculture and Technology till 2015. Since 2015, he has been an associate professor in School of Computer Science and Engineering at the University of Aizu. His research interests include image processing, hardware acceleration, high performance computing, electrical design automation, and combinational algorithms.

Students : B3: Masayuki Tokutake, Ken Watanabe, Shiori Tanikawa, Shuhei Suzuki, Hiroki Ishii, Issei Onodera, Sachi Takahashi, Yoshiaki Ejiri

B4:Yuji Matumoto, Sho Ikeda, Dai Funayama, Shu Takenoshita, Yuma Otsu, Yoshifumi Kato, Yusuke Sekiguchi

M1:Hiroki Saito

Refereed proceedings of an academic conference

[kitamiti-208-033-01:2016] Yoichi Tomioka Hiroki Saito and Junji Kitamichi. Proposing a Highly Reliable Real-Time Operating System for a Processor with a Fault Self-detecting Mechanism. In *13th International Conference on Embedded Software and Systems*, pages pp.164–169, 2016.

Presently, failures and malfunctions of embedded systems can cause serious problems. A highly safe and reliable system requires the ability to deal with failure and malfunction. Furthermore, the sophistication and complexity of real-time systems are increasing with the evolution of technology. We propose a highly reliable real-time operating system (RTOS). The proposed RTOS has a fault detection function for the MicroController Unit (MCU) for real-time applications. This paper reports on the development of an extended function and a fault detection function for RTOS for high-reliability systems. A self-test function of a system and a function that improves the reliability of the MCU are offered. Application Programming Interfaces (APIs) have been developed for fault detection. By developing and running application programs on the system with the developed RTOS, we confirm that the developed RTOS startups and switches multi-tasks and executes cyclic tasks by external timer interrupts. The fault detection function is evaluated using developed application programs. By evaluating the results, we confirm the reliability of the system by the self-test function.

[ytomioka-208-033-01:2016] Chikaaki Kodama Shigeki Nojima Yoichi Tomioka, Tetsuaki Matsunawa. Lithography hotspot detection by two-stage cascade classifier using histogram of oriented light propagation. In *Asia and South Pacific Design Automation Conference*, pages 81–86, 2017.

In advanced semiconductor-process technology, the ability to detect and repair lithography hotspots, which can affect printability, is essential. In this paper, we propose a two-stage cascade classifier for accurate hotspot detection. Our classifier uses a novel layout feature based on the propagation of light passing through a photomask. We performed experiments to evaluate our cascade classifier by applying it to the ICCAD-2012 CAD contest problem. The hotspot detection performance was evaluated according to two indices: (I1) the number of correctly detected hotspots over the number of actual hotspots and (I2) the number of correctly detected hotspots over the number of false hotspots. The results showed that the proposed method gained a 1.1524.4 times improvement

in I2 on average compared to existing state-of-the-art methods, even the one with the best I1.

[ytomioka-208-033-02:2016] Chikaaki Kodama Shigeki Nojima Yoichi Tomioka, Tetsuaki Matsunawa. Lithograpy Hotspot Detection using Histogram of Oriented Light Propagation and Two Staged Cascade Classifier. In *Design Automation Conference (Work-in-Progress poster session)*, June 2016.

(only poster presentation)

Unrefeered proceedings of an academic conference

[kitamiti-208-033-02:2016] IPA(Information technology Promotion Agency) SEC(Software Reliability Enhancement Center) Software Reliability Enhancement Promotion Committee System Fault Diagnosis WG. System Fault Diagnosis Methods for Large and Complicated Embedded Systems / Proposal of Post hoc V&V by Model Base Approach. In *System Fault Diagnosis Methods for Large and Complicated Embedded Systems / Proposal of Post hoc V&V by Model Base Approach*, 2017.

[ytomioka-208-033-03:2016] Hitoshi Kitazawa Shota Saito, Yoichi Tomioka. Source Camera Identification based on Feature Points of PRNU Noise. In *IEICE Tokyo branch student committee workshop*, Janurary 2017.

(In Japanese)

[ytomioka-208-033-04:2016] Hitoshi Kitazawa Daichi Aihara, Yoichi Tomioka. Human Tracking for Sparse Distributed Cameras Considering Overlapping and Separation. In *IEICE Tokyo branch student committee workshop*, January 2017.

(In Japanese)

[ytomioka-208-033-05:2016] Hitoshi Kitazawa Daichi Aihara, Yoichi Tomioka. Human Tracking with Sparse Distributed Cameras

by Spatial- Temporal Likelihood. In *the Media Computing Conference*, June 2016.

(In Japanese)

Research grants from scientific research funds and public organizations

[ytomioka-208-033-06:2016] Hitoshi Kitazawa Yoichi Tomioka. Establishment of Robust Source Camera Identification Technologies for Digital Images, JSPS KAKENHI under Grant 26330152, 2014–2016.

[ytomioka-208-033-07:2016] Yoichi Tomioka Hitoshi Kitazawa. A study on deep learning hardware based on synchronous shift data transfer, JSPS KAKENHI Grant Number 26330060 (co-researcher), 2014–2016.

Academic society activities

[kitamiti-208-033-03:2016] Kitamichi J., 2016.

Member. IEEE

[kitamiti-208-033-04:2016] Kitamichi J., 2016.

Member, IPSJ

[kitamiti-208-033-05:2016] Kitamichi J., 2016.

Member, IEICE

[kitamiti-208-033-06:2016] Kitamichi J., 2016.

Member and Editorial Committee Member, IEICE. Steering Comittee Member, Tohoku Branch, IEICE

[kitamiti-208-033-07:2016] Kitamichi J., 2016.

System Fault Diagnosis WG Member,Software Reliability Enhancement Center (SEC) , IPA

[ytomioka-208-033-08:2016] Yoichi Tomioka, 2016.

Technical Comittee member of IEICE Reconfiguarable System

Advisor for undergraduate research and graduate research

[kitamiti-208-033-08:2016] Ryohei Yamauchi. Acceleration of Algorithm for Minimum p-Quasi Clique Cover Problem using Intel AVX, University of Aizu, 2016.

Thesis Advisor: J. Kitamichi

[kitamiti-208-033-09:2016] Sho Ikeda. Acceleration of Neural Network Algorithm for Fixed Channel Assignment Problem in Cellular Radio Net- works Using CUDA, University of Aizu, 2016.

Thesis Advisor: J. Kitamichi

[kitamiti-208-033-10:2016] Yuji Matsumoto. An Implementation of High-Speed Template Matching usign SoC FPGA, University of Aizu, 2016.

Thesis Advisor: J. Kitamichi

[kitamiti-208-033-11:2016] Dai Funayama. Modeling and Verification of Safety Embedded Systems at Abstract Level using LTSA, University of Aizu, 2016.

Thesis Advisor: J. Kitamichi

[ytomioka-208-033-09:2016] Shu Takenoshita. Scaling Factor Estimation Method Using Three Peak Frequencies Relating to Periodic Interpolation Artifacts, School of Computer Science and Engineering, March 2017.

[ytomioka-208-033-10:2016] Yoshifumi Kato. Robust PRNU Noise Estimation to Noise Contamination by Scene Contents, School of Computer Science and Engineering, March 2017.

[ytomioka-208-033-11:2016] Yuma Otsu. A Study on Feature Extraction Methods for Icy Road Detection from a Single Camera Image, School of Computer Science and Engineering, March 2017.

[ytomioka-208-033-12:2016] Yusuke Sekiguchi. A Study on Memory-Efficient HOG Features for Reliable Human Detection, School of Computer Science and Engineering, March 2017.

Preparation of course examination to measure comprehension

[ytomioka-208-033-13:2016] Entrance exam preparer, checker, evaluator

Did you participate in Faculty Development? (Yes or No) If yes, please describe what you did.

[ytomioka-208-033-14:2016] Planning and management of FD lectures

Did you participate in Public Lectures, and/or Open Campus? (Yes or No) If yes, please describe what you did.

[ytomioka-208-033-15:2016] Tow open off-campus lecture, Open lecture, Open lab in Summer, Open Lab in Autumn