LSI Design Laboratory

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Tsuneo Tsukahara:

Software-Defined Radio Transceivers

Related to this topic, the following work was done in 2017.

A High-Precision Quadrature Modulator and High-Performance RF Front-End Circuits suitable for Multi-band Wireless Transceivers:

Recently the demand for wireless systems such as sensor networks has been rapidly growing. However, radio-wave resources are limited and invaluable especially in these days. Therefore, software-defied radios (SDRs) and cognitive radios, which is a principal application of SDR, can be the key to greatly improving frequency-spectrum efficiency. SDRs demand flexibility and reconfigurability in RF (Radio Frequency) circuits. Therefore, a spectrum-efficient wireless transceiver architecture is indispensable. In this research, we proposed a multi-band wireless transceiver using a high-precision complex quadrature modulator (HP-CQMOD) and a flexible-filtering receiver suitable for sensor networks. As the final goal of our research, we would like to establish a reconfigurable wireless communicator, whose frequency band can be changed according to communication conditions and/or regulations using reconfigurable RF and baseband processors and downloadable software. This is a kind of cognitive radios based on SDR (Software-Defined Radios). In recent years, multi-level modulations such as Quadrature Amplitude Modulation (QAM) are or will be used in Wireless LANs, digital TVs, and the 4th-generation cell-phones. So, very small modulation errors of QMOD are strongly demanded. In the 2017, we concentrated on circuit design of low-power HP-CQMODs, RF-band complex bandpass filters, and image-rejection receivers in wireless transceivers. Moreover, we devised and analyzed a low-

distortion rail-to-rail amplifier, and rail-to-rail voltage-controlled oscillators suitable for quadrature LO generation and wireless power transfer.

RF/IF building blocks we designed have three features as follows:

1. Low-power high-precision complex quadrature modulators are developed and designed, featuring a dual-LO switching quadrature mixer and an RF-band complex bandpass filter. Regarding the dual-LO switching quadrature modulator, we made breadboard experiments using commercially available ICs for analog switches and OP amplifiers and confirmed the usefulness of LO-phase error compensation mechanism.
2. Low-distortion and wideband rail-to-rail amplifiers combining with the Cherry-Hooper architecture.
3. Rail-to-rail voltage-controlled oscillators suitable for quadrature LO generation and wireless power transfer applications.
4. A low-voltage operation operational amplifier based on CMOS inverters suitable for complex bandpass filters. .

Yukihide Kohira:

We investigate *design automation methodology for LSI circuits*. Due to the increase of scales of LSI circuits and the decrease of time to market of LSI products, design automation systems are widely used in order to design LSI circuits. Since the performance of LSI depends on the used design automation systems, it is important to develop design automation methodology continuously in order to obtain good products.

Our research interests are design automation for clock synchronous framework and layout design. In 2017, we focused on following two topics.

Post-silicon Delay Tuning

In recent LSI circuits, process variations increase significantly because of the progress of the process technology. The process variations significantly cause delay variations and delay variations affect the performance and the yield of VLSI chips. If the circuit cannot work at the testing process after the fabrication of LSI chips, the circuit can be recovered by adjusting delays of the programmable delay elements. In 2017, we investigated delay turning methods to improve the yield and to reduce the power consumption and published theses in two domestic conferences.

Dynamic Voltage and Frequency Scaling

In recent years, the usage of Arduino has attracted attention for controlling sensor nodes in IoT. Low power is required for sensor nodes and the reduction of the power consumption in Arduino controlling sensor nodes is also required. In 2017, we created an Arduino compatible machine by removing extra elements from Arduino Uno. In addition, we applied Dynamic Voltage and Frequency Scaling (DVFS) to Arduino compatible machines and measured the current and power consumption by changing the power supply voltage and clock frequency. We published a thesis in a domestic conference.

Refereed academic journal

[tsuka-202-034-01:2017] M. Ugajin, T. Sindo, T. Tsukahara, and T. Hiraguri. An (N+N2)-Mixer Architecture for a High-Image-Rejection Wireless Receiver with an N-Phase Active Complex Filter. *IEICE Trans. Fundamentals*, E100-A(4):1008–1014, April 2017.

A High-image-rejection wireless receiver with N-phase active RC complex filter is proposed and analyzed. Signal analysis shows that the double-conversion receiver with (N+N2) mixers corrects the gain and phase mismatches of the adjacent image. The Monte Carlo simulations show that the image rejection ratio of the adjacent image depends almost only on R and C mismatches in the complex filter.

Unrefeered proceedings of an academic conference

[kohira-202-034-01:2017] K. Muroi and Y. Kohira. Programmable Delay Element for Area Reduction on Post-Silicon Delay Tuning. In *2017 Tohoku-Section Joint Convention of Institutes of Electrical and Information Engineers (1G01)*, August 2017.

[kohira-202-034-02:2017] Y. Kohira. A Study for Application of Dynamic Voltage and Frequency Scaling to Arduino Compatible Board. In *IEICE Society Conference (A-6-12)*, volume A, page 55, September 2017.

[kohira-202-034-03:2017] K. Muroi and Y. Kohira. Clustering for Reduction of Power Consumption and Area on Post-Silicon Delay Tuning. In *IEICE Technical Report (VLD2017-107)*, volume 117, pages 109–114, March 2018.

[tsuka-202-034-02:2017] T. Tsukahara, Y. Yuminaka, S. Narahashi, and T. Taya. An Activity Report of the IEEJ Investigation R/D Committee on New Field Development and Solution Technologies of RF Integrated Circuits. In *The Papers of Technical Meeting on Electronic Circuits, IEE Japan*, number ECT-17-070, pages 1–4, July 2017.

[tsuka-202-034-03:2017] S. Takara and T. Tsukahara. Breadboard Experiment of a Dual-LO Switching Quadrature Modulator. In *The Papers of Technical Meeting on Electronic Circuits, IEE Japan*, number ECT-17-071, pages 5–9, July 2017.

[tsuka-202-034-04:2017] M. Hatanaka and T. Tsukahara. A Differential CMOS Cherry-Hooper Amplifier with a Rail-to-Rail Operation. In *The Papers of Technical Meeting on Electronic Circuits, IEE Japan*, number ECT-17-074, pages 21–25, July 2017.

[tsuka-202-034-05:2017] Y. Ishii and T. Tsukahara. Design and Analysis of Quadrature LC Oscillators using Rail-to-Rail CMOS Differential Amplifiers. In *The Papers of Technical Meeting on Electronic Circuits, IEE Japan*, number ECT-17-087, pages 59–63, Aug. 2017.

[tsuka-202-034-06:2017] S. Takara and T. Tsukahara. Design and Analysis of a Dual-LO Switching Quadrature Modulato. In *The Papers of Technical Meeting on Electronic Circuits*, number ECT-18-012, pages 9–13, March 2018.

[tsuka-202-034-07:2017] M. Hatanaka and T. Tsukahara. Stability Design of a CMOS Inverter-Based Broadband Amplifier. In *The Papers of Technical Meeting on Electronic Circuits, IEE Japan*, number ECT-18-017, pages 33–37, March 2018.

[tsuka-202-034-08:2017] E. Takada and T. Tsukahara. Analysis and Design of Passive Image Rejection Mixer for Wide-Band IF Receiver. In *The Papers of Technical Meeting on Electronic Circuits, IEE Japan*, number ECT-18-033, pages 113–117, March 2018.

Research grants from scientific research funds and public organizations

[kohira-202-034-04:2017] Y. Kohira. Grant-in-Aid for Young Scientists (B) from Japan Society for the Promotion of Science (JSPS), 2017-2020.

Academic society activities

[kohira-202-034-05:2017] Y. Kohira, 2017.

Treasurer, IEEE CEDA All Japan Joint Chapter

[kohira-202-034-06:2017] Y. Kohira, 2017.

Committee Member, IEICE Technical Committee on VLSI Design Technologies (VLD)

[kohira-202-034-07:2017] Y. Kohira, 2017.

Associate Editor, IEICE Trans. Fundamentals

[kohira-202-034-08:2017] Y. Kohira, 2017.

Committee Member, IEICE Tohoku Section

[kohira-202-034-09:2017] Y. Kohira, July 2017.

Guest Editor, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Special Section on Design Methodologies for System on a Chip

[kohira-202-034-10:2017] Y. Kohira, December 2017.

Guest Editor, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Special Section on VLSI Design and CAD Algorithms

[kohira-202-034-11:2017] Y. Kohira, January 2018.

Technical Program Committee Secretary, 23rd Asia and South Pacific Design Automation Conference (ASPDAC 2018)

[kohira-202-034-12:2017] Y. Kohira, January 2018.

Technical Program Committee Member, 23rd Asia and South Pacific Design Automation Conference (ASPDAC 2018), Design for Manufacturability track

[kohira-202-034-13:2017] Y. Kohira, January 2018.

Confirmed Committee Member, ACM SIGDA Student Research Forum at ASPDAC 2018

[kohira-202-034-14:2017] Y. Kohira, March 2018.

TPC Subcommittee Chair, Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2018), Physical subcommittee

[tsuka-202-034-09:2017] T. Tsukaahra, 2017.

Chair of the IEEJ Investigation R/D Committee on High-Performance and Wide-Variation Technologies of High-Frequency Integrated Circuits, IEE Japan, 2017

Advisor for undergraduate research and graduate research

[kohira-202-034-15:2017] F. Sugiyama. Master Thesis: Analytical Pacement Using SPICE Simulator in LSI Circuits, University of Aizu, March 2018.

Thesis Advisor: Y. Kohira

[kohira-202-034-16:2017] R. Azuma. Graduation Thesis: Pixel-based OPC using Quadratic Programming for Mask Optimization, University of Aizu, March 2018.

Thesis Advisor: Y. Kohira

[kohira-202-034-17:2017] K. Muroi. Graduation Thesis: Clustering for Reduction of Power Consumption and Area on Post-Silicon Delay Tuning, University of Aizu, March 2018.

Thesis Advisor: Y. Kohira

[kohira-202-034-18:2017] T. Hoshiba. Graduation Thesis: Acceleration of Analytical Placement by Wire Length Prediction using Machine Learning, University of Aizu, March 2018.

Thesis Advisor: Y. Kohira

[kohira-202-034-19:2017] K. Karahashi. Graduation Thesis: Implementation of AVR Compatible Processor into FPGA in General-Synchronous Framework, University of Aizu, March 2018.

Thesis Advisor: Y. Kohira

[tsuka-202-034-10:2017] Ryota Kobayashi. Graduation Thesis: Design of a Low Distortion Colpitts Oscillator, School of Computer and Science Engineering, Feb. 2018.

[tsuka-202-034-11:2017] Natsumi Abe. Graduation Thesis: A Study of 2-Stage Inverter-Based CMOS Operational Amplifiers, School of Computer and Science Engineering, Feb. 2018.

[tsuka-202-034-12:2017] Shumpei Tosa. Graduation Thesis: A Method of Implementing a Polyphase Filter on a Breadboard, School of Computer and Science Engineering, Feb. 2018.

[tsuka-202-034-13:2017] Naoyuki Sagara. Graduation Thesis: Design of a Low Power Consumption LNA, School of Computer and Science Engineering, Feb. 2018.

[tsuka-202-034-14:2017] Shotaro Nakaya. Graduation Thesis: Comparison and Improvement of Oscillators suitable for Stable and High-Efficient Power Delivery in Wireless Power Transfer Systems, School of Computer and Science Engineering, Feb. 2018.

Others

[tsuka-202-034-15:2017] T. Tsukahara. Fundamentals of Fractional-N Synthesizer. Master Course Lecture, Keio University, Dec. 2017.

[tsuka-202-034-16:2017] T. Tsukahara. Contributions to Research and Development, and the Practical Use of High Frequency Circuits for Digital Wireless Communications, Nov. 2017.

The 31st Radio Engineering and Electronics Association Award, Nov. 7, 2017

Contributions related to regional education

[tsuka-202-034-17:2017] Chair of the Aizu-Area Education and Science Foundation Evaluation Committee