Architecture and Design of an Efficient Router for OASIS 3D Network-on-Chip System

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• Motivation & Research Goal
• TSV Implementation
• Design and Evaluation Results
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Background:  
2D-Network on Chip

• **NoC features:**
  – Simple and scalable architecture.
  – Connects processors, memories and other custom designs together.

• **NoC problems:**
  – When we increase the network size, diameter increases linearly

  An effect on the latency, Throughput, and power consumption
Background:
3D-Network onChip

Fig. 1  3D- Network-on-Chip architecture
[Feero2007, Ben2010]

Reduction of footprint

C : die thickness (0.6 mm)+ intertie distance
Background: 3D-OASIS-Network on Chip

Fig2. 3D-OASIS-Network on Chip architecture

PE: Processor Element  
NI: Network Interface  
R: Router

Wormhole switching  
Stall go flow control  
Mesh topology  
77bit flit format  
Matrix-arbiter scheduler
• TSV (Through Silicon Via) is a vertical connection which is made into silicon.

Fig3. 3D integration with TSVs
Background: Motivation & Research goal

• My research goal is the integration of Through-Silicon-Via (TSV) with 3D-OASIS-NoC(3D-ONoC) router

• Physical implementation of the complete router

• Evaluate the correctness of the proposed router and the hardware complexity using Synopsys Design Compiler
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TSV implementation: 3D-NoC router Design Flow

1. **TSV**
   - Verilog-HDL file
   - Library Exchange Format (LEF) file
   - Liberty Timing (LIB) file

2. **Design compiler** B-2009.09 version
   - Router with TSV NETLIST file (RTL)
   - Router with TSV SDC file

3. **SoC Encounter** 10.1 version
   - Router with TSV NETLIST file (gate-level)
   - Router with TSV SPEF file
   - Router with TSV SDF file

4. **Evaluation**
   - Timing simulation
   - Hardware Design result

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TSV implementation:
3D-ONoC router Architecture

Fig4. 3D-ONoC router with TSV architecture
TSV implementation: TSV LEF file

Making TSV LEF flow

- Library Exchange Format (LEF) file
  - Representing the physical layout (Size, Pin placement, Origin, etc)

FreePDK3D45 using in Tool Virtuoso

Layout

Output LEF file

PDK information needed for designing IC when we use semiconductor process.

Fig5. LEF file information
We make TSV in this information.
TSV implementation:

TSV LEF file

Fig6. Adding Input port to TSV layout
• OBS is a macro obstruction area where no standard cell can be placed.
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Design and Evaluation Results:

Propose 3D-ONoC router design

Fig 7 3D-ONoC router layout: (a) with metal wire (b) without metal wire
Design and Evaluation Results:
Propose 3D-ONoC router design
Design and Evaluation Results:
Post-layout timing simulation

Addr: 000 000 000
Router1

dat_in_local

tsv_up_out -> tsv_down_in

Addr: 000 000 001
Router2

dat_out_local2

Data 21bit 000000_00000000_1100100

<table>
<thead>
<tr>
<th>dat_in_local[37:0]</th>
<th>'b 000000_</th>
</tr>
</thead>
<tbody>
<tr>
<td>tsv_up_out[37:0]</td>
<td>'b 000000_</td>
</tr>
<tr>
<td>tsv_down_in[37:0]</td>
<td>'b 000000_</td>
</tr>
<tr>
<td>dat_out_local2[37:0]</td>
<td>'b 000000_</td>
</tr>
</tbody>
</table>

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**Design and Evaluation Results:**

<table>
<thead>
<tr>
<th>Evaluation parameter</th>
<th>Nangate 45nm, FreePDK3D45</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clock</strong></td>
<td>450 MHz</td>
</tr>
<tr>
<td><strong>Voltage</strong></td>
<td>1.1 V</td>
</tr>
<tr>
<td><strong>TSVs</strong></td>
<td>156</td>
</tr>
<tr>
<td><strong>TSV size</strong></td>
<td>4.06 ( \mu \text{m} \times 4.06\mu \text{m} )</td>
</tr>
<tr>
<td><strong>TSV Pitch</strong></td>
<td>15 ( \mu \text{m} )</td>
</tr>
<tr>
<td><strong>Keep-out-Zone</strong></td>
<td>10 ( \mu \text{m} )</td>
</tr>
<tr>
<td><strong>flit size</strong></td>
<td>38 (payload: 21) bit</td>
</tr>
</tbody>
</table>
### Design and Evaluation Results: Hardware design results

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of pins</strong></td>
<td>557</td>
</tr>
<tr>
<td><strong>Power (uW)</strong></td>
<td>408</td>
</tr>
<tr>
<td><strong>Chip size</strong></td>
<td>350um × 350um</td>
</tr>
<tr>
<td><strong>Area (um²)</strong></td>
<td></td>
</tr>
<tr>
<td>Router</td>
<td>19132 (33%)</td>
</tr>
<tr>
<td>TSV</td>
<td>38000 (67%)</td>
</tr>
</tbody>
</table>
# Design and Evaluation Results:
## Hardware design comparison results

<table>
<thead>
<tr>
<th>System/Parameter</th>
<th>Area (μm)</th>
<th>Power (μW)</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline router</td>
<td>16880</td>
<td>341</td>
<td>645.1</td>
</tr>
<tr>
<td>Proposed router</td>
<td>57132</td>
<td>408</td>
<td>450</td>
</tr>
</tbody>
</table>

- 338% increase
- 19.6% increase
- 30.2% decrease
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Conclusion and Future Work

• In this research, I proposed the integration of TSVs with 3D-ONoC router design.

• The TSV component was designed using several CAD tools and according to the norms used in current technology.

• The post-layout simulation showed the freeness of the proposed router from any logical errors or timing violations.
Conclusion and Future Work

- From the hardware design and evaluation results we found out that the proposed router's exhibits an area of \(57132\mu m^2\), the power consumption is \(408\mu W\), and the frequency is 450MHz.
- Design and Evaluation of larger network-size(5×5×5) with larger application
- Consider fault-tolerance in the proposed router
Thank you for listening!