PHENIC: Silicon Photonic 3D-Network-on-Chip Architecture for High-performance Heterogeneous Many-core System-on-Chip

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Abstract—Network-on-chip architectures can improve the scalability, performance, and power efficiency of general multi-processor systems and application-specific heterogeneous multicore and many-core SoCs (MCSoCs). This interconnection paradigm when combined with 3D integration technology offers advantages over 2D NoC design, such as shorter wire length, higher packing density, and smaller footprint.

However, as processor architects and semiconductor industries are heading towards complex and large system design consisting of hundreds of PEs, traditional design approaches may not be enough for providing significant large bandwidth with low-power consumption.

Optical Network-on-Chip (ONoC) promises significant advantages over their electronic counterparts. In particular, they offer a potentially disruptive technology solution with fundamentally low power dissipation that remains independent of capacity while providing ultra-high throughput and minimal access latency.

In this work, we propose a novel 3D Optical Network-on-Chip, named PHENIC 3D-ONoC, based on our earlier proposed 3D OASIS-NoC\(^1\). We present architecture, hardware design, and preliminary evaluation results in a fair amount of details.

**Keywords**—optical interconnects; 3D-NoC; Many-core SoCs; Architecture, Heterogeneous Systems.

I. Introduction

Embedded systems are moving towards the integration of hundreds of cores on a single chip and hold the promise of increasing performance through parallelism. As the number of cores integrated into an embedded chip increases, the on-chip communication becomes power and performance bottleneck in current and future embedded applications (cell phone, video, ...).

Network-on-Chip (NoC) architecture [1], [2], [3] has been proposed as a viable solution to meet the performance and design productivity requirements of these complex systems. In addition to simplifying the design of conventional systems, NoC has been also proposed to address other design/performance challenges, such as scalability, and wire delay problems.

In recent years, many researchers [5], [28], [29], including our group [3], [4], investigated the architectures and design of two-dimensional electronic NoCs based on various types of topologies, flow-controls, and routing algorithms.

There have been also enormous efforts in 3D integration and 3D-NoCs designs to further address the interconnection delays problem and also the integration of disparate signals (analog, digital, or rf) or technologies (SoI, SiGe, HBTs, or GaAs) [27], [6]. By providing a third dimension of interconnect, wire delays can be substantially reduced. In addition, because for many high-performance applications, the performance bottleneck is often in the chip-to-chip or chip-to-memory communication, 3D integration offers the real advantage that massive amounts of bandwidth can be provided between device layers. This was helped by the recent advances in 3D integration technology in the area of heat dissipation cooling mechanisms, and through-silicon vias (TVSs), which cut across thinned silicon substrates to establish inter-die connectivity after die-bounding.

However, most proposed 2D/3D NoC architectures use copper based electrical interconnects as the physical level to transfer information between different components. Unfortunately, with DSM VLSI technologies, it is becoming increasingly difficult for copper based electrical interconnects to satisfy the design requirements of delay, power, and delay uncertainty [6], [31], [24], [5]. As a result, copper-based architecture may not scale beyond several tens of cores.

Future high-performance chips are expected to combine hundreds of components each integrated together to satisfy large and complex applications’ power and performance requirements. Thus, to achieve significant and scalable solution to the interconnect delay problem, real fundamental changes in system interconnect, and fabrication technologies are needed.

Optical interconnect is an attractive solution for achieving ultra-high communication bandwidth in long-distance communication networks. However, this solution has not yet been widely investigated in chip-to-chip or in on-chip interconnections.

As the individual performance of main photonic devices

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(i.e. photodetectors, modulators, waveguides, and lasers) significantly improves recently, there is a growing interest in addressing the issues of photonic and CMOS devices integration [13], [14], and new applications for a converged electronic-photonic IC platforms are being developed [15], [16], [17], [18], [19].

Optical Network-on-Chip (ONoC) is a novel concept enabling high bandwidth using Wavelength Division Multiplexing (WDM). Optical switch and waveguides are used to realize the same function as a conventional electrical router but with routing based on wavelengths and with no need for an arbiter. The routing and flow control are managed in electronics.

ONoC offer a potentially disruptive technology solution with fundamentally low power dissipation that remains independent of capacity while providing more bandwidth at near-speed-of-light transmission latency.

The key power saving in ONoC based systems comes from the fact that once a photonic path is established, the optical data are transmitted end to end without the need for buffering, repeating, or regenerating [34], [33], [37], [39], [24], [25], [26]. This is different from electronic NoCs, where message are buffered, regenerated and then transmitted on the inter-router links several times en route to their destination [37]. In addition photonic routers do not need to switch with every bit of the transmitted data like in electronic routers; optical routers switch on and off once per message, and their energy dissipation does not depend on the bit rate. This feature allows the transmission of ultra high bandwidth messages while avoiding the power cost which found in traditional electronic networks [37].

In this work, we propose architecture and preliminary evaluation results of a new 3D photonic NoC (PHENIC 3D-ONoC) for application specific many-core SoCs (MCSoC). PHENIC architecture is based on our earlier proposed electronic 3D-OASIS Network-on-Chip (OASIS 3D-NoC) [10], [9], [7], [8].

II. PHENIC OPTICAL ROUTER ARCHITECTURES

The most prevalent photonic network element of PHENIC architecture is the non-blocking seven-port bidirectional router, which dynamically routes broadband messages to their destinations. Microresonator (MR) is used as a simple component to implement the basic 1 x 2 switching element.

A given MR element has a resonance wavelength \( \lambda_{mr} \), which is determined by the material and structure of the microresonator. When the wavelength \( \lambda_{mr} \) of a given optical signal is equal to the resonance wavelength \( \lambda_{mr_{res}} \) of the microresonator, the optical signal will make turn as shown in Fig. 1 (left). Otherwise, it will pass by the microresonator and will continue on the same direction (Fig. 1 (right)). PHENIC’s optical router block diagram is shown in Fig. 2. It is based on multiple optical switching elements and consists of a switching unit (SU) and control unit (CU) modules. The SU is a simplified module of the typical 7 x 7 crossbar The control unit is made up of a centralized control unit (CU) and 7 (one for each direction: EAST, WEST, NORTH, SOUTH, UP, DOWN) control (EOC/OEC) interfaces (Gateways). The CU uses electrical signals to configure the switching fabric via an electronic network according to the routing requirement of each packet (discussed later).

PHENIC system also consists of electrical routers which are mainly responsible for routing control packets and configuring the optical switching fabric by electrical signals.

III. SYSTEM ARCHITECTURE

PHENIC architecture realizes the same functions as classical electrical NoC (i.e. our earlier developed 3D-OASIS-NoC [10], [9], [7], [8]) but with routing based on wavelength. It consists of two different network layers. The upper layer is the Photonic Communication Layer (PCL) and is based on silicon broadband photonic switches interconnected by waveguides. The PCL integrates an optical data transmission network for optical payload packets transmission. The bottom layer is called Electronic Control Layer (ECL) and contains an electrical control network for routing packets and configuring the network. The ECL uses electrical signals for configuration by mainly powering on or off the MRs of the PCL network. It is based on conventional CMOS transistors and was built in hardware.

PHENIC architecture is based on 3D-Mesh topology for interconnecting several tiles. Each PE is connected to a gateway which enables the electro-optical conversion as shown in Fig. 3. The gateways consists of two parts: core-to-network module (C2N) and network-to-core N2C) module. The C2N module is composed of a serializer, drivers, lasers, and multiplexer. While the N2C is composed with demultiplexer, PIN photo-diodes. Each transmitter core consists of laser(s), drivers and a serializer, trans-impedance amplifier (TIA), and deserializer (DES).

A. OPTICAL PATH SETTING

Before sending the optical data packets (Payload), the source node (transmitter) first issues a configuration or path setting packet via a Copper Based Electrical Link (CBEL) to the destination node (receiver). The configuration packet is routed in the electronic control network (ECN), reserving the photonic switches along the path for the photonic message
which will follow it. It includes a destination address information, and other additional control information. The routing is based on our LAFT (Look Ahead Fault Tolerant) routing algorithm [9]. LAFT performs the routing decision for the next node taking into consideration its electrical link status and selects the best minimal path. In order to deliver any control flit from source to destination nodes, LAFT assumes that the links connecting the components to the local input and output ports are always non-faulty, and there exists at least one minimal path between a [Src, Des] pair (discussed later in more details).

When the destination node receives the configuration packet, it will acknowledge that the optical path setup is done. In order to fully utilize the capability of the implemented bidirectional optical waveguides, the receiver sends a small light pulse back to the sender on the optical waveguide. When the small ACK pulse is received and processed, the source node, then, starts transmission of optical data packets via the waveguides (Fig. 1 (a)). Finally, when the transmission is finished, the reserved path would be released (tore down) by a release packet. This approach is similar to the circuit switching scheme in which the path is first reserved before payload transmission. By using such communication protocol, no buffer is needed for the optical data and also the latency performance is guaranteed. Data in PHENIC arrives at the destinations in the same order as they are generated and, so, there is no need to reorder packets at the destination nodes.

B. PHENIC Photonic Building Blocks

Lasers, modulators, and waveguides are all passive elements. Below, we describe these components in details.

1) Laser Source: Since there is no available high-speed, electrically driven, on chip monolithic laser light [5], [12], PHENIC uses an off-chip laser sources, such as VCSEL (Vertically Cavity Surface Emitting Laser). As indicated in Fig. 1(c), the off-chip laser source provides light to the modulator, which transducers electrical information into a modulated optical signal. Then, when the lights enter the chip, optical splitters and waveguides route it to the different modulators used for data transmission.

2) Modulators: Before messages are transmitted on the PCL network, the electrical messages from each component should be converted to optical form. PHENIC implements at each node a Network Gateway (EOC/OEC) serving as a photonic network interface based on silicon optical modulators [48] or Mach-Zehnder silicon modulators [12] and SiGe photodetectors [49], [12].

To reduce conversions time, the modulator should be small (i.e. the circular shaped 10µm ring-modulator [22]) and fast.
The performance of the above modulators is dependent on the on-to-off light intensity ratio [5], which depends on the electrical input signal strength. A higher extinction ratio is better and required for fast and accurate signal detection. Works in [22], [5] reported that an extinction ratio greater than 10dB is high acceptable and enough to enable proper signal detection without causing communication errors.

3) Waveguide: The waveguides provide the physical interconnection between all sources and destinations and enables connectivity between all photonic devices in PHENIN systems. As shown in Fig. 1 (c), the transmitter demultiplexes the light into appropriate wavelength channels and then modulates each of the channel with a digital data stream generated by the electronic component to be interconnected (Fig. 1 (b)). Finally, photonic signals are routed to various PEs via routers and waveguides. Here, we have to note that the refractive index [5] of the waveguide material has a big impact of the bandwidth,
latency, and area of an optical interconnect. A waveguide typically has a width of 0.3μm [35].

Once the photonic signals are received by the destination node, the signals must be converted back to electrical form by the gateway unit, which uses a photodetector (i.e., P-I-N diode [51], [5]) and a trans-impedance amplifier (TIA) devices to perform this task. In addition, since PHENIC simultaneously transmits different wavelengths per waveguide (bidirectional), a wave selective filter for each received wavelength is needed at the destination node (receiver).

4) Microring Resonator Active Elements: The main element of PHENIC and other silicon photonic systems is the microring resonators (MRs) (see Fig. 1 (a)). MRs are capable of effectively guiding the path an optical signal will take through careful design of the dimensions and position of the resonator. Optical signals couple into ring resonators at specific regularly spaced wavelengths in the optical spectrum, called resonant modes [54].

C. Routing Algorithm

As we mentioned in the previous section, the communication path should be acquired first before sending the photonic signals (payload) on the PCL network. This operation requires the configuration packet (CP) to travel a number of electronic routers and undergo some routing decision in each hop. Additionally, the CP may experience blocking (i.e., due to some faults) at certain points in its path further contributing to the setup latency.

Once the path is acquired, the transmission latency of the optical data is very short and depends only on the group velocity of light in a silicon waveguide (approximately $6.6 \times 10^7 m/s$ for a 2-cm path crossing a chip [51]).

The path-setup procedure is based on our earlier proposed LAFT routing algorithm [9], [7], [8]. LAFT performs the routing decision for the next node taking into consideration its channel status and selects the best minimal path. The above routing scheme is illustrated in Algorithm 1. In the first phase, LAFT calculates the next node address depending on the next-port identifier read from the flit. For a given node wishing to send a flit to a given destination, there exist at most 3 possible directions through X, Y, and Z dimensions, respectively. In the second phase, LAFT performs the calculation of these 3 directions by comparing x, y and z coordinates of both current and destination nodes concurrently. At the same time, as these directions are being computed, the fault-control module reads the next-port identifier from the flit and sends the appropriate fault information to the corresponding input-port. By the end of this second phase, LAFT has information about the next node fault status and also the three possible directions for a minimal routing. In the next phase, the routing selection is performed. For this decision, we adopted a set of prioritized conditions to ensure fault-tolerance and high performance either in the presence or absence of faults:

1) The selected direction should ensure a minimal path, and it is given the highest priority in the routing selection.
2) We should select the direction with the largest next-hop path diversity.
3) The congestion status is given the lowest priority.

Depending on these priorities, LAFT reads the fault status of the next node received from the fault-control module and checks the number of possible non-faulty minimal directions. As illustrated in Algorithm 1, if only one non-faulty minimal direction is obtained, this direction will be selected as out-port for the next node. If more than one possible minimal direction is available, the algorithm selects the direction which leads to a node with higher path diversity. The diversity value for a given node is the number of possible directions leading to the destination through a minimal path [32]. A node with high diversity results in more routing choices. This means that the probability of finding a non-faulty link is greater when considering faults. When no faults are detected in the system, selecting the direction with the highest diversity gives more choices to find the least congested direction.

To obtain directions with high diversity, we should select those leading to nodes located in the center of the mesh and avoid routing to the edges of the network (similar approach was introduced in [32]). When the three possible directions are minimal and have the same diversity, the routing selection is made depending on the congestion of each output port. This congestion information is obtained by the stop signal issued from the flow control used in our 3D-OASIS-NoC system. When there is no valid minimal route available, LAFT chooses a non-minimal route while also considering the 2nd and 3rd priorities (path diversity and congestion) as illustrated in algorithm 1.

IV. Related Work

Due to technology limitation, photonic NoC architecture is bufferless in the foreseeable future. The circuit-switched nature of photonic interconnect directly affects the performance and power characteristics of on-chip communication. Briere et al. [34] proposed a multistage ONOC with a passive switching router. Kirman et al. [33] presented a hierarchical optical bus for multiprocessor systems. The optical loop encircles the chip with wavelength division multiplexing support at the top level of the hierarchy. Shacham et al. [37] presented an optical NoC architect re based on augmented-mesh and a blocking $4 \times 4$ optical switch. The network is circuit-switched and some critical network design issues such as path-setup and tear-down are covered in the work. Beausoleil et al. [36] proposed a crossbar based ONOC, where 64 wavelengths are multiplexed over 270 waveguides. In [11] proposed to use an optical ring waveguide with bus protocol standards to replace global pipelined electrical...
Pan et al. [52] presented a high throughput optical crossbar-based on-chip network architecture with localized arbitrations. Cianchetti et al. [39] presented an optical network with a predecoded source routing mechanism. Low latency is achieved by transmitting packets several hops in a single clock cycle if no contention exists. Gu et al. [45] proposed a fat-tree based ONoC. In [40], Kodi et al. proposed an ONoC architecture for 64 cores. The bandwidth is maximized with the proposed static routing and wavelength allocation schemes. In [41], Ding presented an optical routing framework to reduce the power consumption of ONoCs. Batten et al. [42] proposed an optical mesh based on a hybrid optical-electrical global crossbar, where the processing cores and DRAM are divided into sub-meshes and connected with the optical crossbar. In [43], silicon MRs of small size have been demonstrated. The fabrication is based on silicon waveguides with a cross-section of 500-200 nm and the insertion loss is about 0.5 dB.

Experiment results show that the MR on/off switching power consumption is on the order of 20µW [44]. Ji et al. [46] presented a non-blocking 5 × 5 optical router. The router uses 16 MRs in total. One MR should be turned on for every switching, except for switchings from east to south, or south to east, or west to north, or north to west.

There are also several works about electronic 3D-NoCs. In [9], a so called OASIS 3D-NoC based on mesh topology and look-ahead fault tolerant (LAFT) routing algorithm was designed and prototyped in FPGA. Feero et al. [47] evaluated the performance of 3-D electronic NoCs with 3-D mesh and fat-tree topologies. It was found that the 3-D realization of both mesh and fat-tree based NoCs could improve the performance significantly with higher integration densities and smaller footprints. In [50], Chen et al. proposed a 3-D NoC architecture based on De-Brujin-Graph to achieve smaller network diameter and smaller network latency.

In addition to researches about electronic 3D-NoCs, there are also several research works on the 3D-ONoC architectures. Gu et al. [45] proposed a 3-D optical cubic-mesh NoC together with an optimized partial crossbar based optical router. In [24], [25], [26], authors proposed the design of passive routing 6 × 6 and 7 × 7 optical routers and propose optimized floor-plans for the 3-D mesh-based ONoCs.

V. Conclusion

This report presented PHENIC 3D-ONoC architecture description. It also presented a detailed survey about existing ONoC architectures.

VI. Future Work

- Optical router performance and complexity evaluations
- Electronic control layer complexity evaluation
- PHENIC power consumption evaluation.
- other.

References


