SYA14 - Neuromorphic Computing

Lab 2

1 Objective

In this lab, we will design neurons in Python and Verilog HDL. The following two neurons will be designed:

- Leaky Integrate and Fire
- Izhikevich

Note: The Verilog HDL versions should be designed in a cost-efficient manner. Therefore, they should have some differences in comparison to the Python models.

2 Prerequisite

The following are the prerequisites of this exercise:

- Python and Jupyter Notebook.
- Verilog HDL.
- Modelsim with command line (see Lab 1).
- Familiar with CAD tool to export: area cost, timing, and power consumption.

3 Ex 2.1: Neuron Design

3.1 LIF

Theoretically, LIF neuron operations are expressed in the following equation:

$$V_i(t) = V_i(t-1) + \sum_j w_{i,j} \times x_j(t-1) - \lambda \tag{1}$$

where $w_{i,j}$ is the synaptic weight between the i^{th} neuron and the j^{th} one. $V_i(t)$ is the membrane potential of i^{th} neuron at the t timestep and $x_j(t-1)$ is the output pre-synaptic spike of i^{th} neuron and the leaky value λ, respectively. This output of the i^{th} neuron is expressed with the equation below.

$$x_i(t) = \begin{cases} 1, \text{ if } V_i(t) \geq V_{th}, \\ 0, \text{ otherwise.} \end{cases} \tag{2}$$

The Jupyternotebook of LIF neuron can be downloaded from `https://web-ext.u-aizu.ac.jp/misc/neuro-eng/book/NeuromorphicComputing/lab/lif_book-ver.ipynb`

3.2 Izhikevich

The Izhikevich neuron can be found at `https://www.izhikevich.org/publications/spikes.htm`. Figure1 summarizes the Izhikevich model and equation.

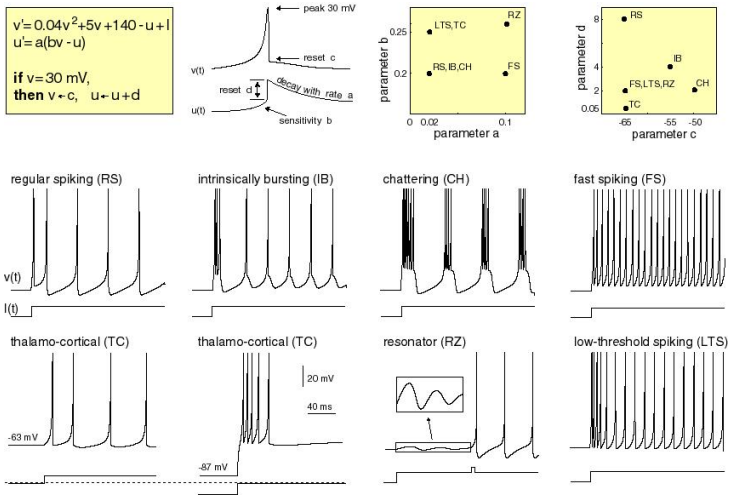

Figure 1: The design of Izhikevich neuron.

In terms of equations, the original Izhikevich model is

$$v' = 0.04v^2 + 5v + 140 - u + I$$

$$u' = a(bv - u)$$

Then, the Euler's method is applied:

$$v[t+1] = v[t] + h(0.04v[t]^2 + 5v[t] + 140 - u[t] + I[t])$$

$$u[t+1] = u[t] = a(bv[t] - u[t])$$

where t is the time step.

The Jupyternotebook of the Izhikevic neuron can be downloaded from `https://web-ext.u-aizu.ac.jp/misc/neuro-eng/book/NeuromorphicComputing/lab/izhik_tonic-spiking.ipynb`

3.3 Exercise content

Run the example source code and report the result.

4 Ex 2.2: RTL design

Based on the design of Ex 1.1, design RTL architecture of LIF and Izhikevich neuron with the following constraints:

- Synchronous clock with a reset signal.
- The bit-width: Membrane potential 16-bit, synaptic weight 8-bit, other parameters 16-bit.

Report the simulation results and compare between RTL and the Python model.

5 Submission format and Deadline

Your report should be prepared in English and should contain the following:

1. Your name, your ID, and the Lab #.
2. All reports
3. Submission format: soft copy.

Note: This Laboratory is designed for the book [1]

[1] Book: Neuromorphic Computing Principles and Organization 1st, Edition, ISBN-10: 3030925242, ISBN-13: 978-3030925246, Publisher: Springer, May 2022.