

Advanced Computing Systems Laboratory

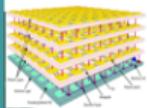
**Power/Energy-
Efficient Computing
Systems**



**Brain-inspired
Algorithms &
Systems**



**Advanced On-chip
Interconnects
& 3D-ICs**



**Green
Computing**



BEN-DANG-WANG Laboratory
School of Computer Science and Engineering
The University of Aizu

MEMBERS/メンバー紹介

Faculty/教授 ([SMM repository](#))



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Research Areas

研究分野

The rapidly advancing field of computing technology demands continuous innovation to meet the growing needs of society while ensuring sustainability and energy efficiency. The ACS Lab stands as a pioneering research facility dedicated to the advancement of computing technologies. Serving as a collaborative hub for students, faculty, and industry partners, our mission is to transform high-power, general-purpose computing into low-power, domain-specific solutions. Our primary focus lies in the research and development of innovative architectures and edge solutions, aiming to enhance computational efficiency and performance while significantly reducing energy consumption. Notably, our groundbreaking contributions in the design and optimization of high-performance, energy-efficient computing systems have made a substantial impact, particularly in areas such as compute, network, and high-availability workloads.

Our research is currently dedicated to addressing these critical challenges by focusing on four main research topics: Energy Efficient Computing Systems, Brain-Inspired Chips and Systems, Advanced On-Chip Interconnects, and Green Computing. Through a multidisciplinary approach, we aim to develop cutting-edge solutions that enhance computing performance, reduce environmental impact, and pave the way for sustainable technological advancement.

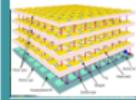
Power/Energy-Efficient Computing Systems



Brain-inspired Algorithms & Systems



Advanced On-chip Interconnects & 3D-ICs



Green Computing



Low-power Neuromorphic SoC 低消費電力ニューロモーフィック SoC

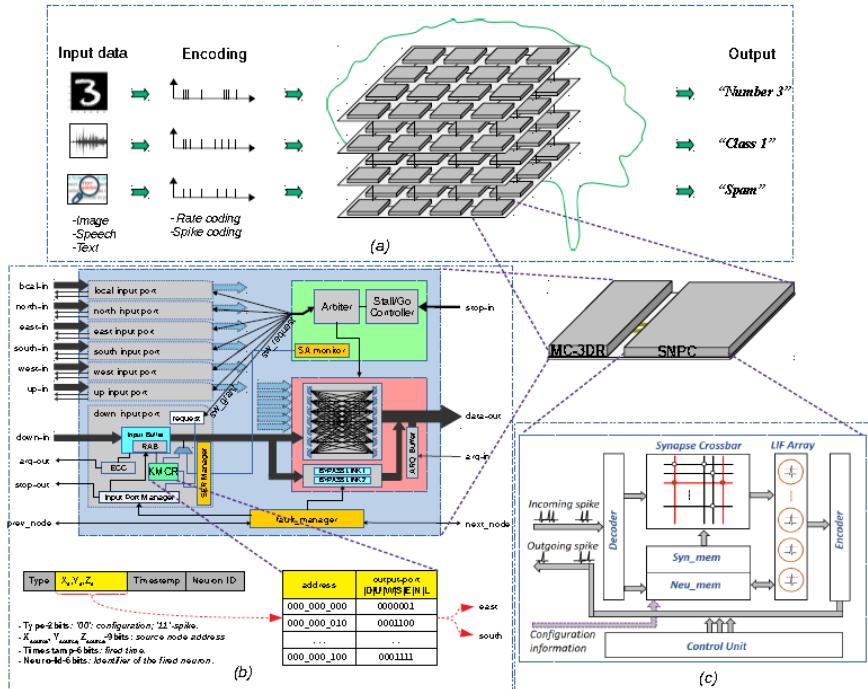
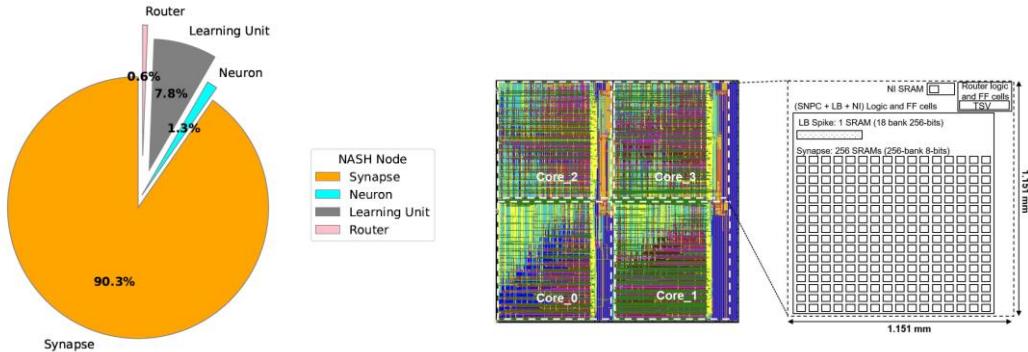


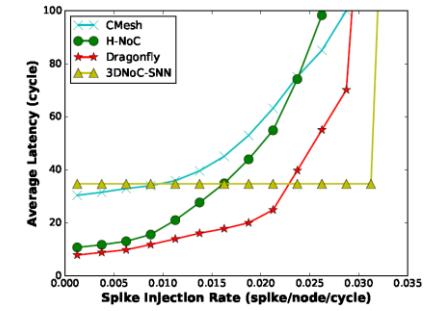
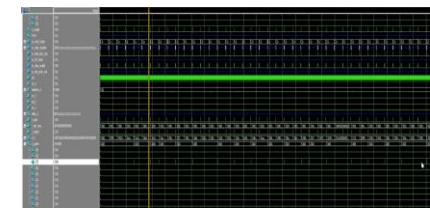
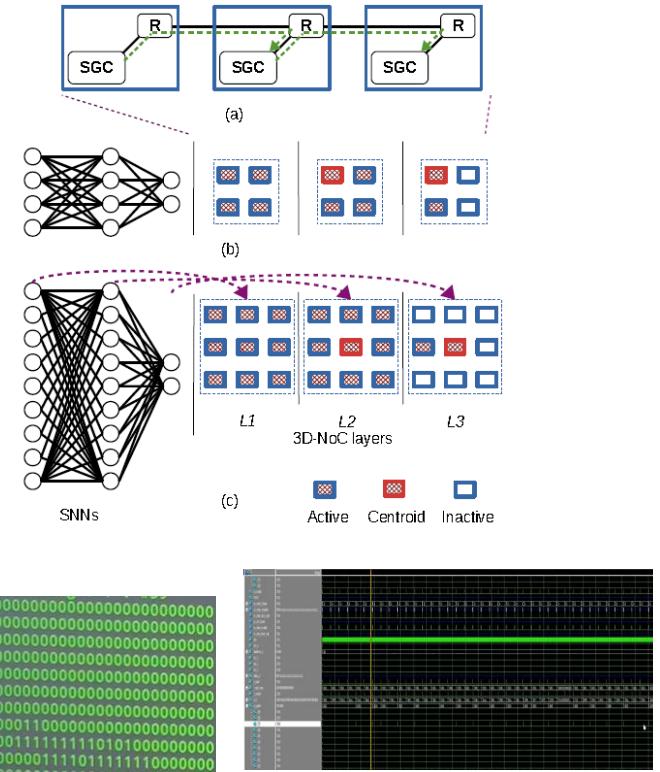
Fig. 5: System architecture: (a) 3DNoC-SNN organization, (b) Multicast router architecture (MC-3DR), (c) Spiking neuron processing core (SNPC).



Area analysis of a NASH node

Parameter/System	XY-UB	XYZ-UB	SP-KMCR		FTSP-KMCR	
Architecture	Baseline	NASH	Baseline	NASH	Baseline	NASH
Area (mm^2)	1.312	1.316	1.322	1.322	1.320	1.325
Power (mW)	66.16	66.63	66.50	66.84	68.22	70.10

Design complexity comparison of NASH and Baseline nodes

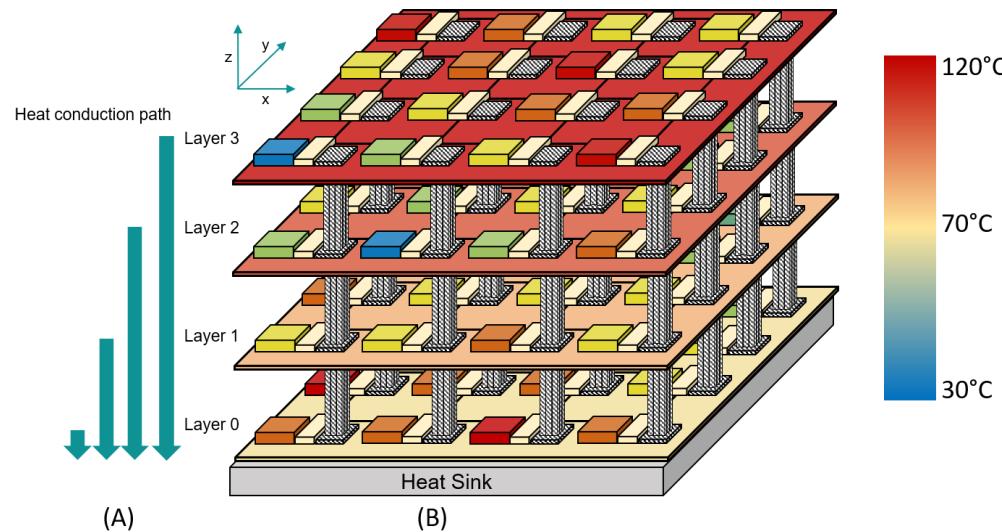


Evaluation Result, Average latency evaluation, and comparison over various SIRs

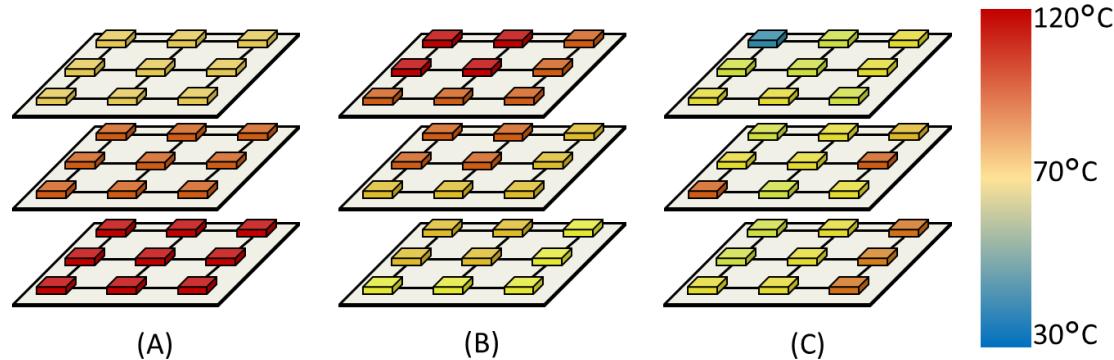
O. M. Ikechukwu, K. N. Dang and A. Ben Abdallah, "On the Design of a Fault-Tolerant Scalable Three Dimensional NoC-Based Digital Neuromorphic System With On-Chip Learning," IEEE Access, vol. 9, pp. 64331-64345, 2021, doi: 10.1109/ACCESS.2021.3071089

A1

Thermal-Aware Mapping Method for 3D-NoC Neuromorphic System



(A) shows the difference in the Heat conduction path to the heat sink between the layers. (B) Represents an illustration of the temperature in each layer and neurons cluster



Different temperature scenarios, (A) Hot layer.(B) Hotspot in one layer.(C) Moderated temperature

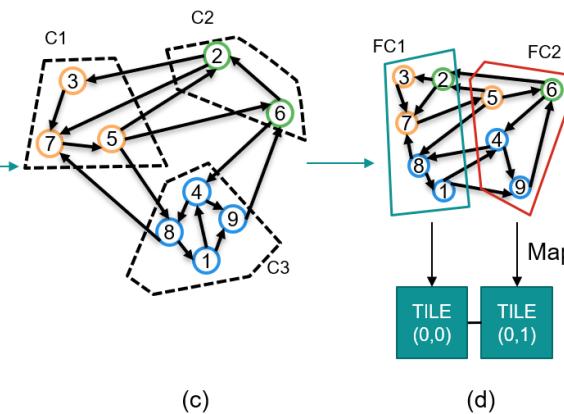
Thermal-Aware Mapping Method for 3D-NoC Neuromorphic System

N	T1	T2	T3	T4	T5
1	0	0	1	0	1
2	0	1	0	0	1
3	1	0	0	1	0
4	1	0	1	0	0
5	1	0	1	1	0
6	0	0	0	0	1
7	1	1	0	1	0
8	0	0	1	0	1
9	1	0	1	0	1

(a)

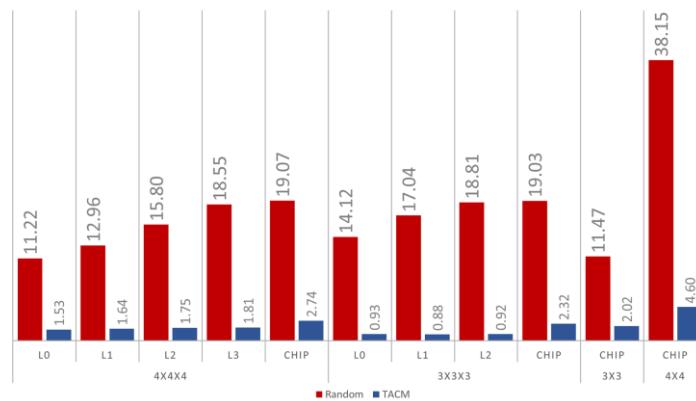
C1	C2	C3
4	1	1
4	1	3
0	3	2
2	3	1
1	4	2
3	0	3
1	4	4
4	1	1
3	2	0

(b)



(d)

Illustration of an example of the TACM method. (a) represents a sample of neuron activity. (b) is the difference between the neurons activities and the centroids. (c) is the resulting clusters from (b). (d) represents the re-clustering to the final clusters and map them to the tiles



Maximum and minimum temperature difference for the different architectures between the tiles within the layers and the whole chip for the lowest maximum temperature case

Tile: 030 Temp: 352.80 K	Tile: 130 Temp: 352.03 K	Tile: 230 Temp: 352.03 K	Tile: 330 Temp: 350.94 K
Tile: 020 Temp: 354.35 K	Tile: 120 Temp: 353.82 K	Tile: 220 Temp: 353.82 K	Tile: 320 Temp: 353.15 K
Tile: 010 Temp: 354.35 K	Tile: 110 Temp: 353.82 K	Tile: 210 Temp: 353.82 K	Tile: 310 Temp: 353.15 K
Tile: 000 Temp: 355.54 K	Tile: 100 Temp: 354.92 K	Tile: 200 Temp: 354.92 K	Tile: 300 Temp: 354.29 K

(a)

Tile: 030 Temp: 356.15 K	Tile: 130 Temp: 355.36 K	Tile: 230 Temp: 355.36 K	Tile: 330 Temp: 340.79 K
Tile: 020 Temp: 373.87 K	Tile: 120 Temp: 367.47 K	Tile: 220 Temp: 367.47 K	Tile: 320 Temp: 347.16 K
Tile: 010 Temp: 373.87 K	Tile: 110 Temp: 367.47 K	Tile: 210 Temp: 367.47 K	Tile: 310 Temp: 347.16 K
Tile: 000 Temp: 378.94 K	Tile: 100 Temp: 371.09 K	Tile: 200 Temp: 371.09 K	Tile: 300 Temp: 355.23 K

(b)

Highest maximum temperature of the 4x4 2D-NoC chip for the two different mappings: (a) is from TACM method. (b) is from a random mapping method

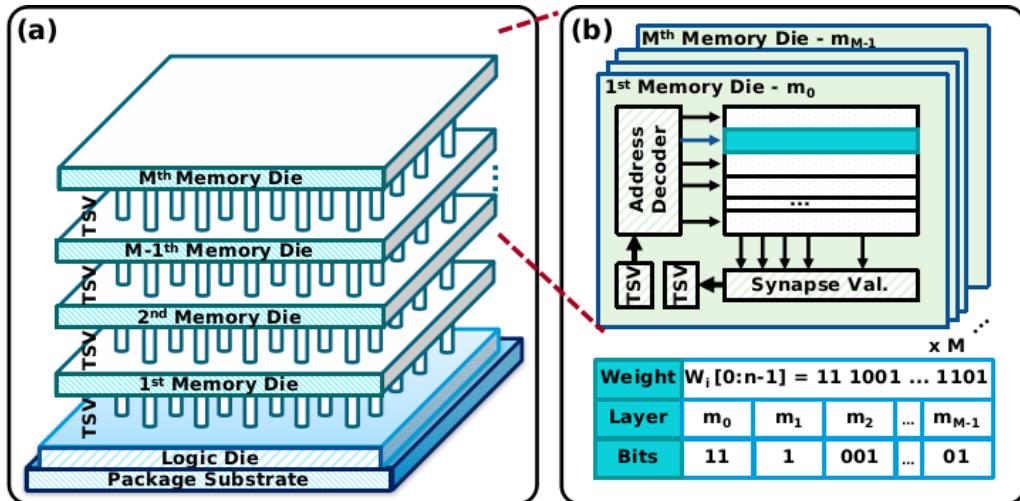
References:

- [1] M. Maatar, K. N. Dang, and A. B. Abdallah, "Thermal-aware task- mapping method for 3d-noC-based neuromorphic systems," in 2023 6th International Conference on Electronics Technology (ICET), 2023, pp. 1067–1076

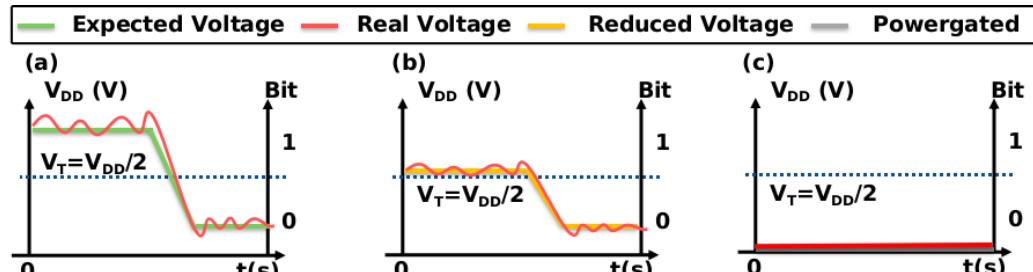
A3 3-D IC-based Stacking Synaptic Memory for Spiking Neural Networks

| スパイキング・ニューラル・ネットワークのための3次元ICベースのスタッキング・シナプティック・メモリー

The idea is to distinguish the critical levels of synaptic weights and then isolate them using stacking layers of 3-D architectures. Hence, applying the low-power techniques for low-important bits to gain power efficiency.

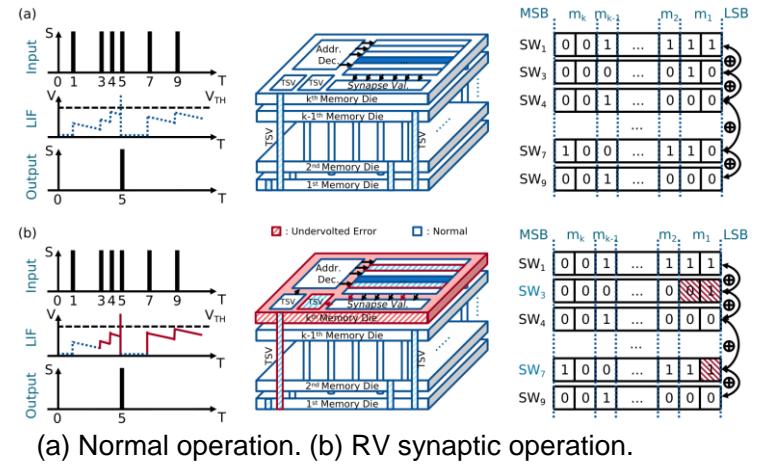


(a) 3次元構造。 (b) ビット配置。



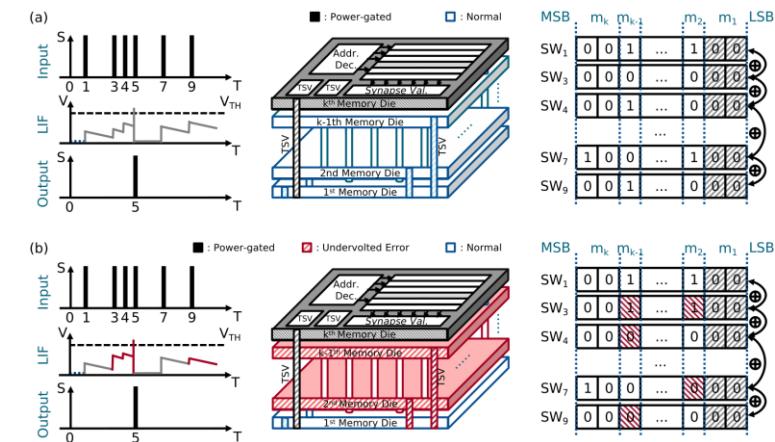
(a) Normal operation. (b) RV operation. (c) PG operation.

(a) 通常動作。 (b) RV動作 (c) PG動作。



(a) Normal operation. (b) RV synaptic operation.

(a) 通常動作。 (b) RV動作。

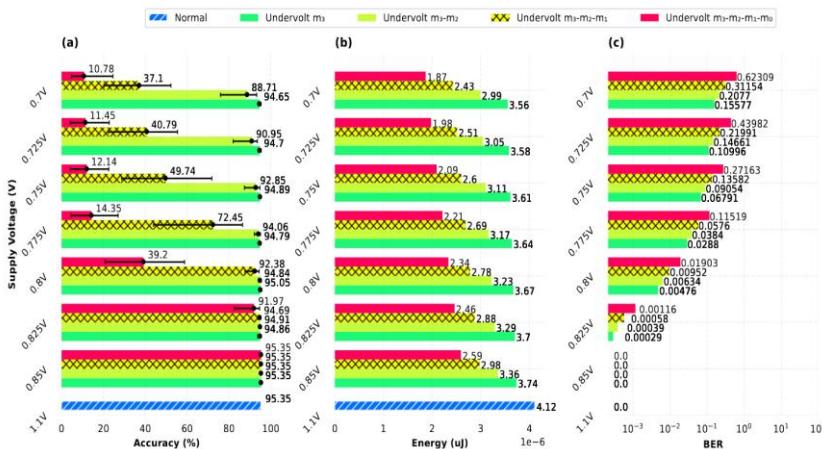


(a) PG operation. (b) PG & RV synaptic operation.

(a) PG動作。 (b) PG & RV動作。

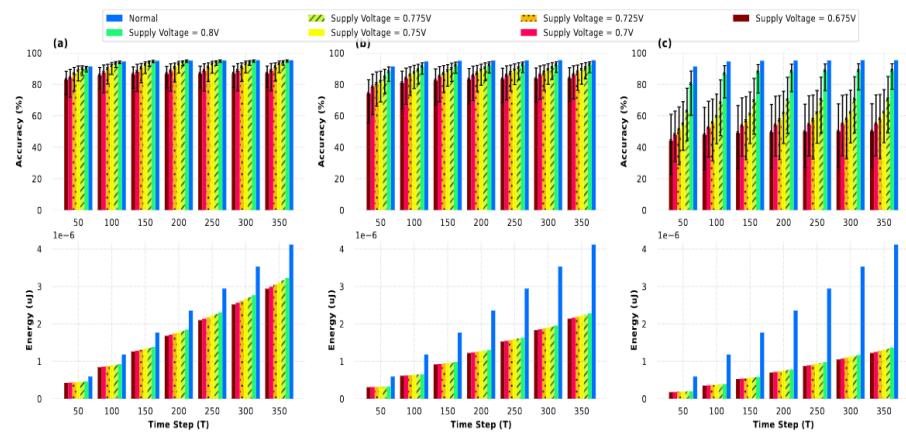
A3 3-D IC-based Stacking Synaptic Memory for Spiking Neural Networks | スパイキング・ニューラル・ネットワークのための3次元ICベース のスタッキング・シナプティック・メモリー

MNIST dataset - Three perception layers of SNN [784 48 10]
 • MNIST データセット・SNN の 3 つの認識層 [784 48 10]



(a) Accuracy. (b) Energy consumption. (c) Bit-Error-Rate.

(a) 精度。 (b) 消費エネルギー。 (c) ビットエラー率。



Accuracy vs Energy with RV & PG:

- (a) RV 2 layers.
- (b) PG 1 layer & RV 2 layers.
- (c) PG 2 layers & RV 2 layers.

精度 vs エネルギー・RV & PG:

- (a) RV 2層。
- (b) PG 1層 & RV 2層。
- (c) PG 2層 & RV 2層。

References:

[1] N.-D. Nguyen and et al., "Power-aware Neuromorphic Architecture with Partial Voltage Scaling 3D Stacking Synaptic Memory", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, doi: 10.1109/TVLSI.2023.3318231.

[2] N.-D. Nguyen and et al., "An In-Situ Dynamic Quantization With 3D Stacking Synaptic Memory for Power-Aware Neuromorphic Architecture," in IEEE Access, vol. 11, pp. 82377-82389, 2023, doi: 10.1109/ACCESS.2023.3301560.

(a) PG動作。 (b) PG & RV動作。

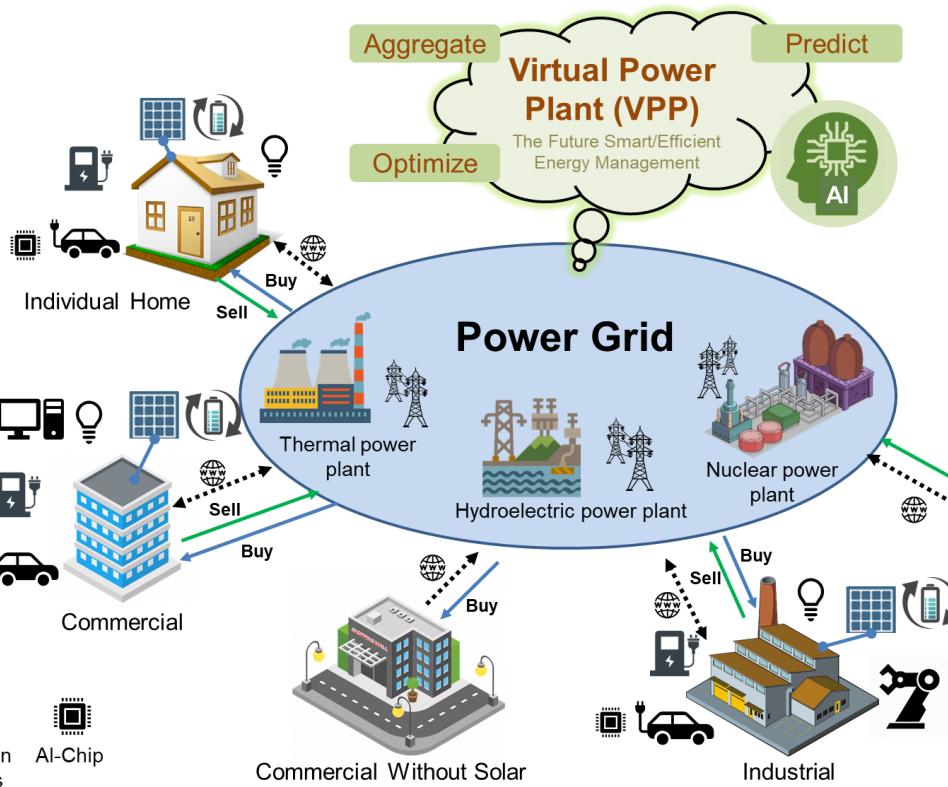
Off-Grid Energy Storage Solar Carport オフグリッドエネルギー貯蔵ソーラーカーポート

Optimized Energy Distribution for a Cleaner, Greener Energy Future

VPP is a digital platform that links decentralized energy resources across different locations in Japan and optimizes energy usage.

 Communication (Internet)
 Data / Information exchange
 Green energy transmission
 Energy transmission

		
Solar Panel	Renewable Source	Computer
		
Electric Vehicle	EV Charging Pile	Industrial Machine
		
Common Utilities	AI-Chip	

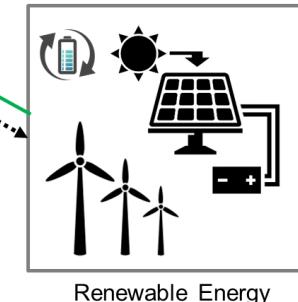


Advantages:

Intelligent – Electricity produced from different sources can be coordinated intelligently as a “single producer”

Reliable – Energy fluctuations (e.g. due to solar intermittency) can be stabilized automatically.

Resilient – Localized faults can be isolated, minimizing impact to consumers.



Z. Wang, M. Ogbodo, H. Huang, C. Qiu, M. Hisada, A. Ben Abdallah, "AEBIS: AI-Enabled Blockchain-based Electric Vehicle Integration System for Power Management in Smart Grid Platform," IEEE Access, vol. 8, pp. 226409-226421, 2020, doi:10.1109/ACCESS.2020.3044612.

Off-Grid Energy Storage Solar Carport オフグリッドエネルギー貯蔵ソーラーカーポート

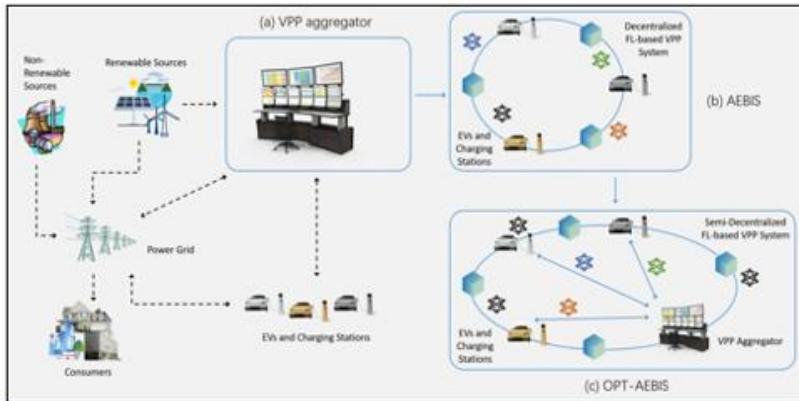


Fig. 1. Virtual Power Plant (VPP): (a) conventional VPP aggregator, (b) AEBIS, (c) optimized AEBIS (O-AEBIS).



Fig. 5. A demonstration of the energy management system based on our system named AEBIS and its optimized version O-AEBIS.

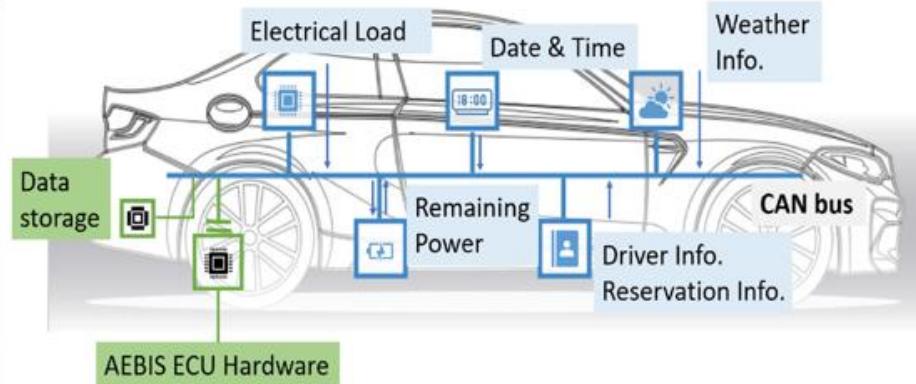
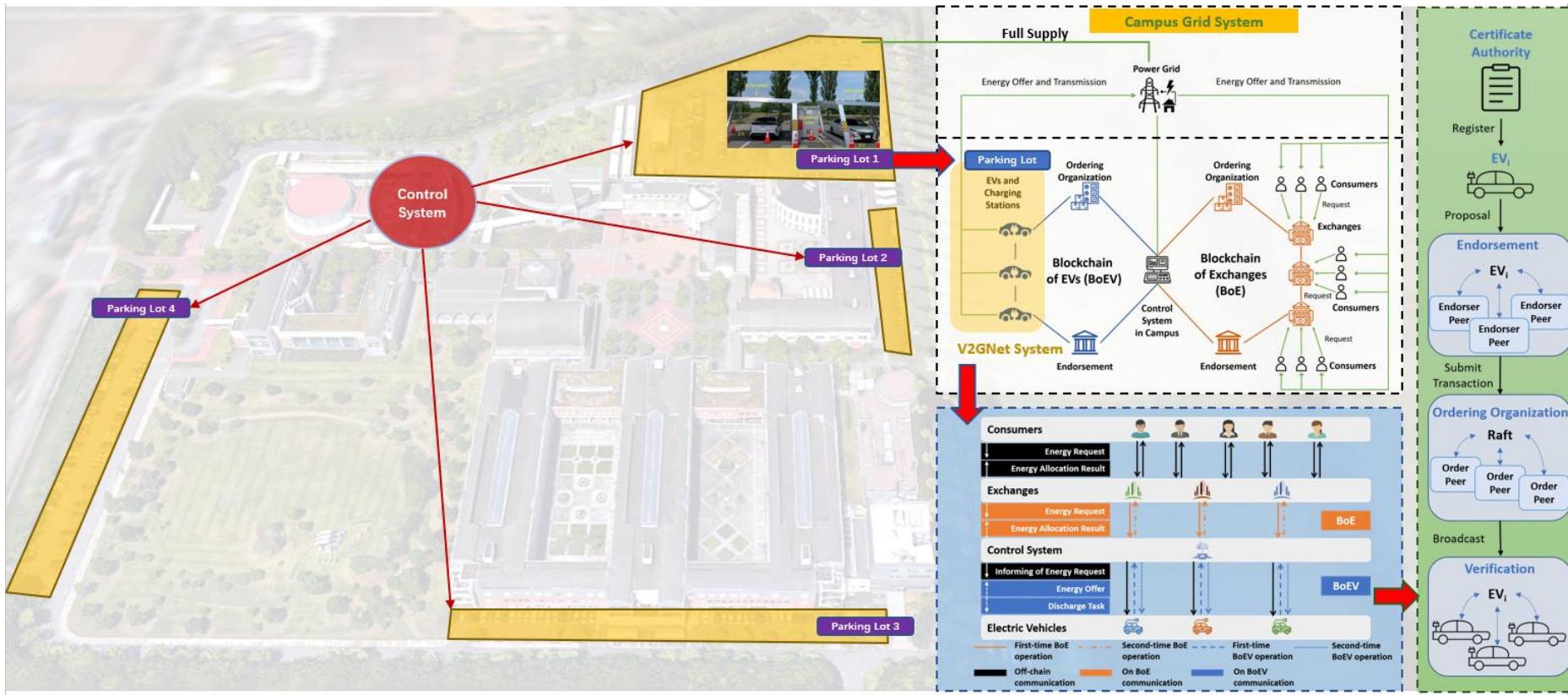


Fig. 2. Neural Network for Power Consumption Prediction of Electric Vehicle (EV).

Name	BRAM_18K	DSP48E	FF	LUT
Expression	-	-	0	493
Instance	-	5	414	950
Memory	2	-	320	20
Multiplexer	-	-	-	627
Register	-	-	454	-
Total	2	5	1188	2090
Available	120	80	35200	17600
Utilization (%)	1	6	3	11
Weights	Memory required			
Weights	568 Bytes			
Biases	60 Bytes			
Inputs	44 Bytes			
Total	672 Bytes			

Fig. 6. Hardware complexity of power consumption prediction system on the Zynq-7010 FPGA. The system utilized 3% of the FF, 11% of the LUT, 6% of the DSP48, and approximately 1% 18k BRAM.

Off-Grid Energy Storage Solar Carport オフグリッドエネルギー貯蔵ソーラーカーポート



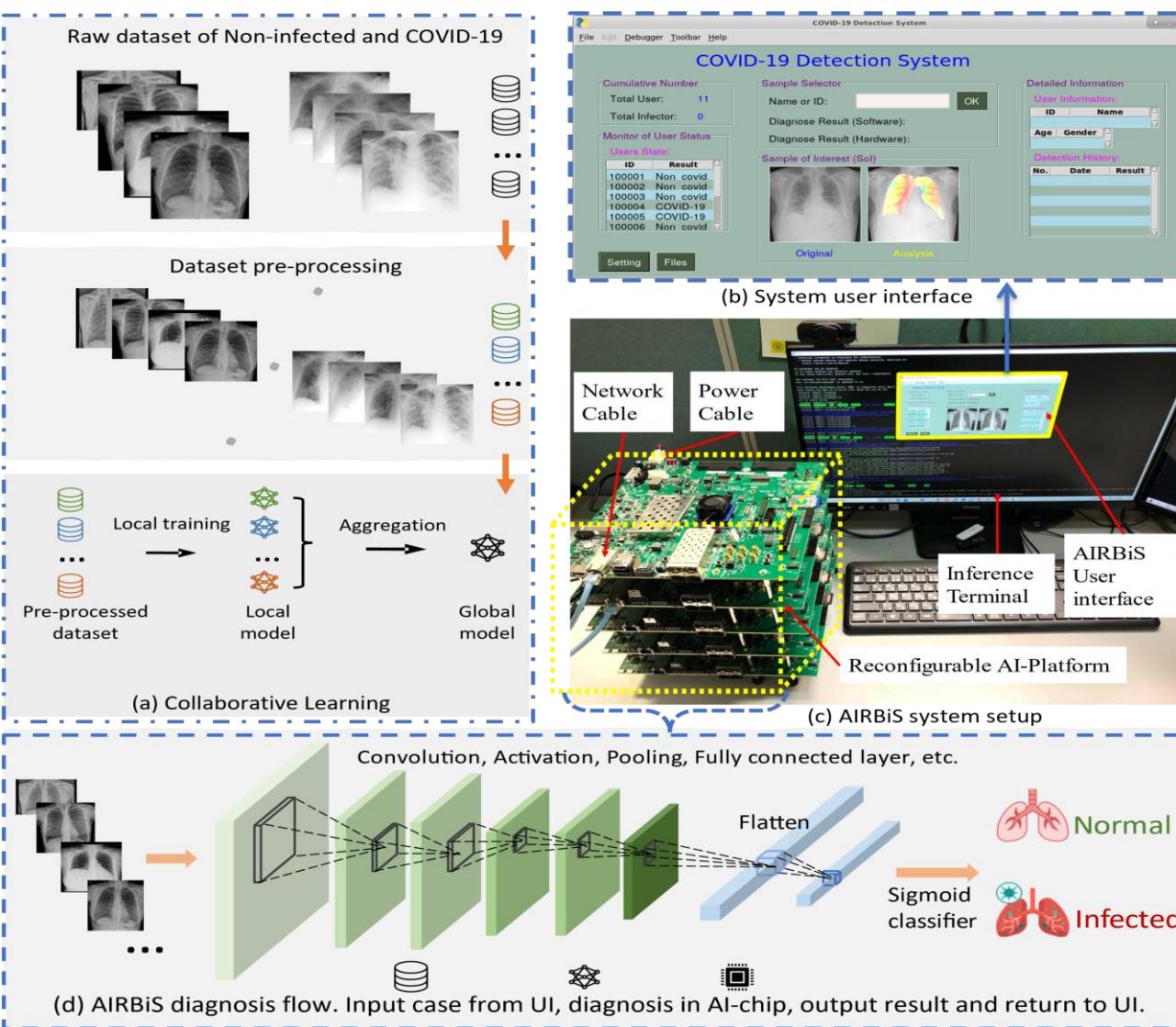
[特許第6804072号] (2020.12.04) ベンアブダラ アブデラゼク (Abderazek Ben Abdallah), 久田雅之, "Virtual Power Platform Control System [仮想発電所制御システム]", 特願2020-033678号 (2020.02.28)

エネルギーの取引方法とシステム/Energy Trading Method and System

Abderazek Ben Abdallah, Wang Zhishang, Masayuki Hisada, "An electricity trading system and an electricity trading method [電力取引システム及び電力取引方法に関する]", 特願2022-022472 Power Consumption Prediction Method and System for Power Management in Smart Grid/ スマートグリッドにおける電力管理のためのEV消費電力予測 方法とシステム

Abderazek Ben Abdallah, Wang Zhishang, Khanh N. Dang, Masayuki Hisada, "EV Power Consumption Prediction Method and System for Power Management in Smart Grid [スマートグリッドにおける電力管理のためのEV消費電力予測 方法とシステム]", 特願2022-022472

A5 AI-Powered Hardware-Software Platform for Pneumonia Detection/ 肺炎検出のためのAIを活用したハードウェアとソフトウェアのプラットフォーム



Resource	Utilization		Available		Utilization (%)	
	ANN	SNN			ANN	SNN
LUT	54,585	27,288	274,080	274,080	19.9	9.9
LUTRAM	3668	2048	144,000	144,000	2.5	1.28
FF	53,035	37,098	548,160	548,160	9.7	6.77
BRAM	824	0	912	912	90.4	0
DSP	35	0	2520	2520	1.4	0
BUFG	4	18	404	404	1.0	4.45
MMCM	1	0	4	4	25	0

Core/Parameter	Area (mm ²)		Power (mW)	
	SNN	ANN	SNN	ANN
Convolution core	0.0748	0.0755	0.007	0.011

Table 7.2. Dataset description.			
Label	Class	Train	Test
COVID	COVID	2870	700
	COVID(Augmented)	14,349	-
Non-COVID	Normal	9791	400
	Lung_Opacity	5762	250
	Viral_Pneumonia	1288	50
	Sum	34,060	1400

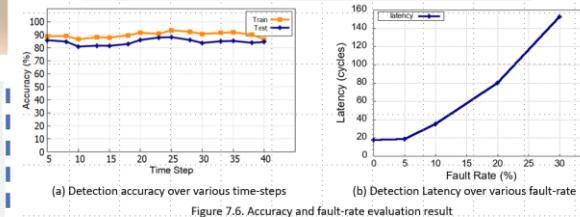


Figure 7.6. Accuracy and fault-rate evaluation result.

Neuromorphic Robot Arm and Prostheses

ニューロモーフィック ロボット アームと義足

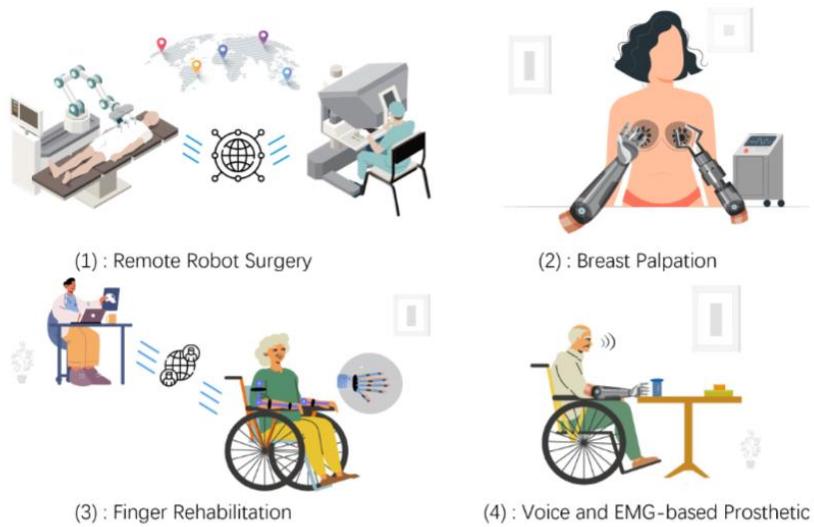
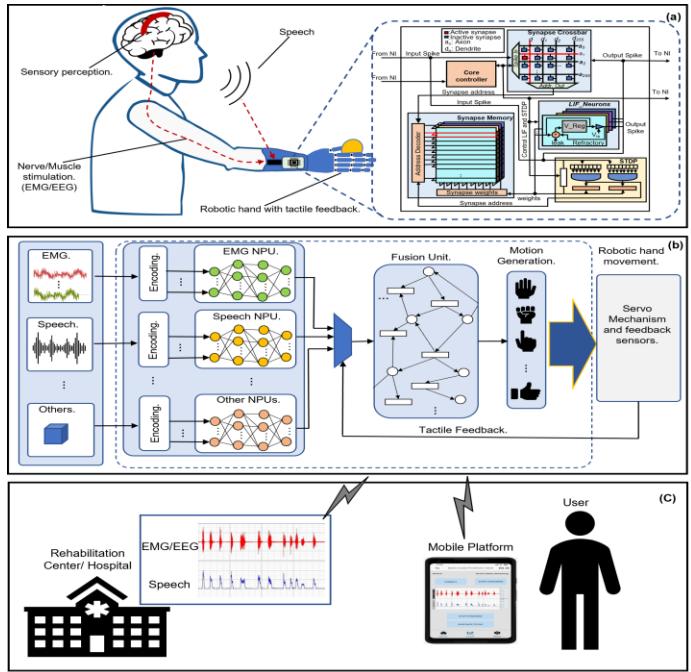


FIGURE 4. The Neuromorphic AIzuHand target applications. (1) Remote Robot Surgery, (2) Breast Palpation, (3) Finger Rehabilitation, (4) Voice and EMG-based Prosthetic Hand.

Abderazek Ben Abdallah, Huankun Huang, Nam Khanh Dang, Jiangning Song, "AIプロセッサ [AI Processor]," 特願2020-194733 (2020年11月24日)



- Device Name: AlzuHand I
- Total Weight: 422g (276g without controller)
- Control: sEMG
- DoF: 5
- Feedback: No
- Related patent: 特願2019-124541
- Contact "benab(at)u-aizu.ac.jp"



AlzuHand for Autonomous Painting

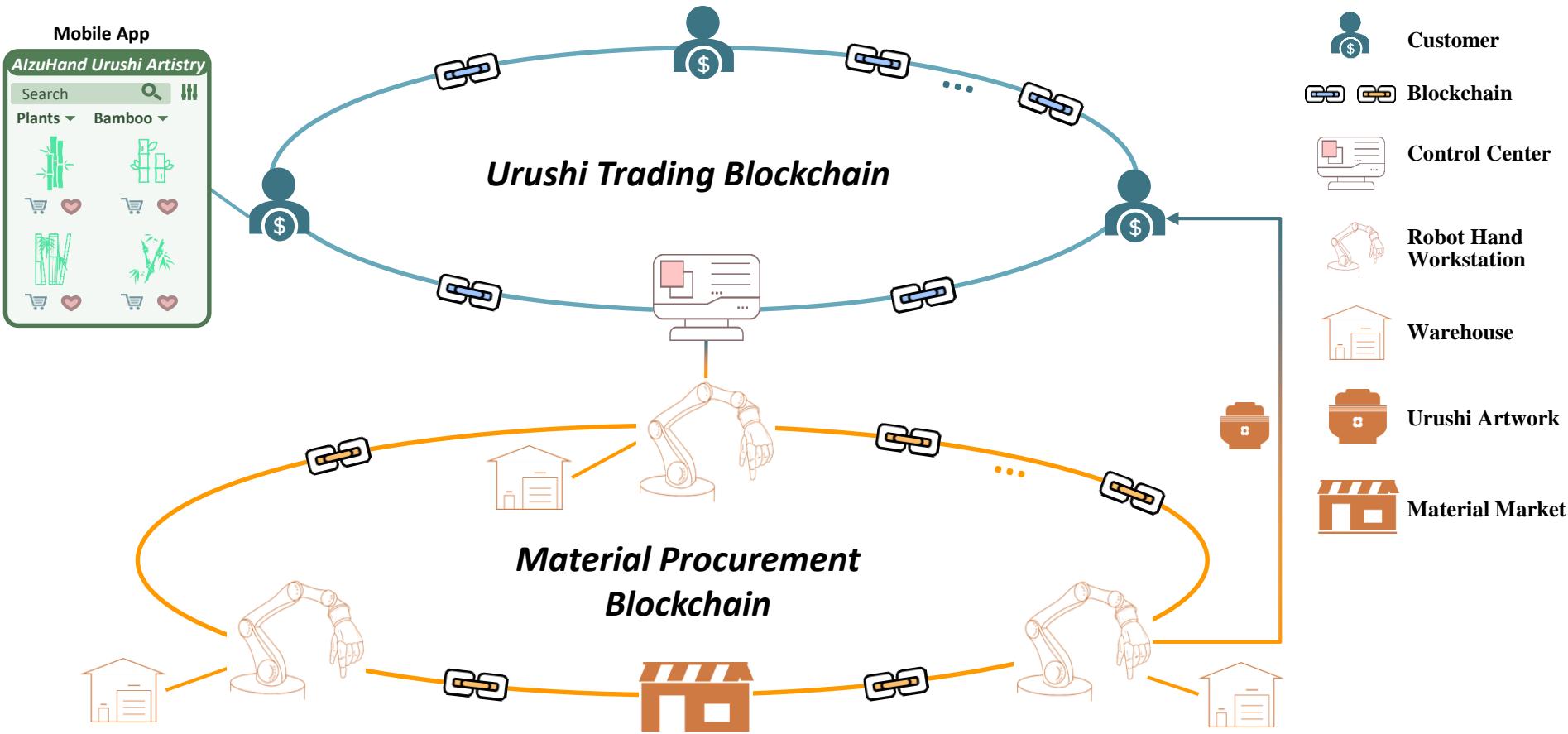


Fig. 1: Overview of The Autonomous Robot Hand Painting Platform and System.

天気図を用いた発電量予測AIモデル

AI model for predicting power generation amount using weather maps

